60V, 3A, Step-Down Converter TD1663

General Description

The TD1663 is a 60V, 3A step down regulator with an integrated high-side MOSFET. With a wide input range from 9V to 60V, it's suitable for various applications from industrial to automotive for power conditioning from unregulated sources. An ultra-low 1μA current in shutdown mode can further prolong battery life. Internal loop compensation means that the user is free from the tedious task of loop compensation design. This also minimizes the external components of the device. A precision enable input allows simplification of regulator control and system power sequencing. The device also has built-in protection features such as cycle-by-cycle current limit, thermal sensing and shutdown due to excessive power dissipation, and output overvoltage protection.

The TD1663 is available in an ESOP-8 package.

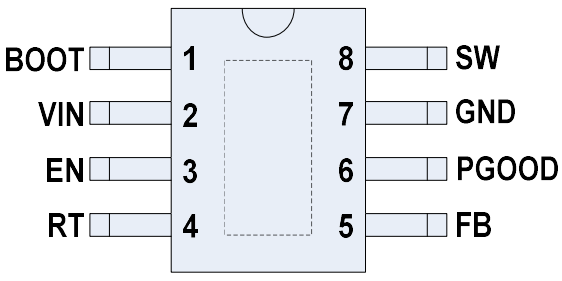
Features

- 9V to 60V Input Range
- 3A Continuous Output Current
- 150 mΩ High-Side MOSFET
- Current Mode Control
- Adjustable Switching Frequency from 200kHz to 1 MHz
- Internal Compensation for Ease of Use
- 1 μA Shutdown Current
- Thermal, Overvoltage and Short Protection
- Available in a ESOP-8 Package

Applications

- Automotive Battery Regulation
- Industrial Power Supplies
- Telecom and Datacom Systems
- General Purpose Wide Vin Regulation

Pin Configurations

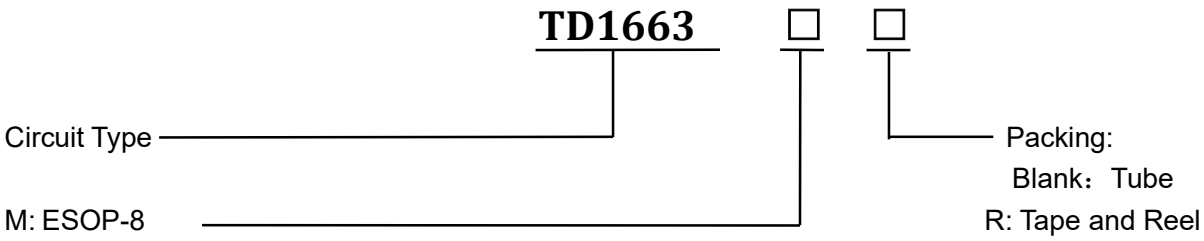


(Top view)

Pin Description

Pin Number	Pin Name	Description
1	BOOT	Bootstrap capacitor connection for high-side MOSFET driver. Connect a high quality 0.1μF capacitor from BOOT to SW.
2	VIN	Connect to power supply and bypass capacitors C_{IN}. Path from VIN pin to high frequency bypass C_{IN} and GND must be as short as possible.
3	EN	Enable Input. Pulling it up above the specified threshold to enable. Pulling this pin below the specified threshold to disable.
4	RT	Resistor Timing. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency.
5	FB	Feedback input pin, connect to the feedback divider to set V_{OUT}. Do not short this pin to ground during operation.
6	PGOOD	Power-Good pin, open drain output for power-good flag, use a 10 kΩ to 100 kΩ pull-up resistor to logic rail or other DC voltage no higher than 7 V.
7	GND	System ground pin.
8	SW	Switching output of the regulator. Internally connected to high-side power MOSFET. Connect to power inductor.
9	Thermal Pad	Major heat dissipation path of the die. Must be connected to ground plane on PCB.

Ordering Information



Function Block

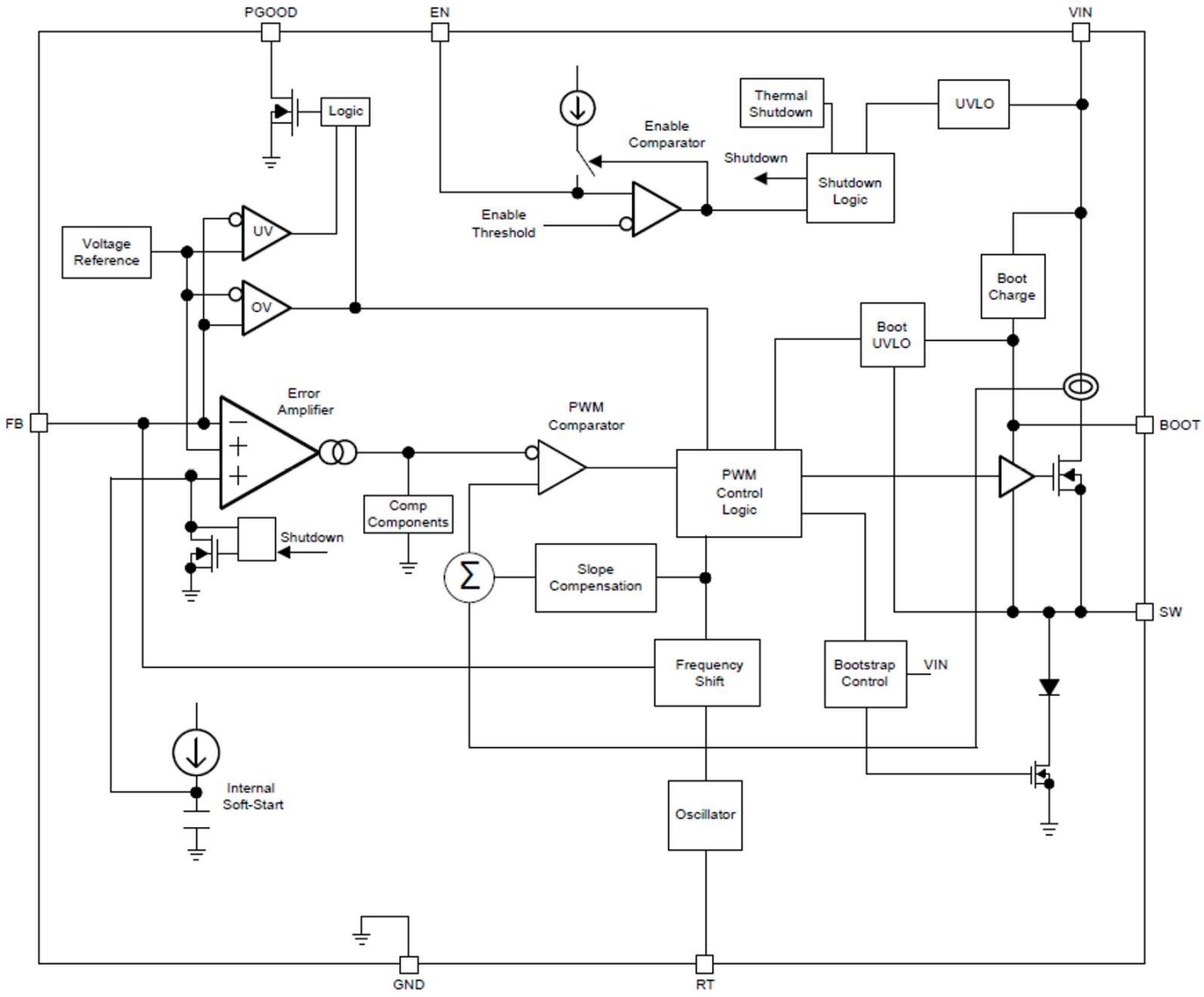


Figure1 Function Block Diagram of TD1663

Absolute Maximum Ratings (Note1)

		Rating	Unit
Input Voltages	VIN to GND	-0.3 to 65	V
	EN to GND	-0.3 to 7	
	PGOOD to GND	-0.3 to 7	
	FB to GND	-0.3 to 7	

Output Voltages	BOOT to SW	6.5	V
	SW to GND	-0.3 to VIN+0.3	
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
θ_{JC}	Thermal Resistance from Junction-to-Case	9	°C/W
θ_{JA}	Thermal Resistance from Junction-to-Ambient	48	°C/W
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-boody model(HBM)	±2000	V

Recommended Operation Conditions

		Range	**Unit**
Buck Regulator	VIN	9 to 60	V
	VOUT	0.8 to 50	
	SW	-1 to 60	
	FB	0 to 5	
Frequency	Switching frequency range	200 to 1000	kHz
Temperature	Operating junction temperature, T_J	-40 to 125	℃

Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits.

For guaranteed specifications, see Electrical Characteristics.

Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of -40 °C to +125 °C, unless otherwise stated.

Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25 °C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply: V_{IN} = 9 V to 60 V.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operation input voltage		9	-	60	V
UVLO	Under voltage lockout thresholds	Rising threshold	-	8.5	-	V
		Hysteresis	-	1.4	-	V
I_{SHDN}	Shutdown supply current	V_{EN} = 0V, T_A = 25°C, 9V≤V_{IN}≤60V	-	1.0	3.0	μA
I_Q	Operating quiescent current (non-switching)	V_{FB} = 1.0V, T_A = 25°C	-	200	-	μA
ENABLE (EN PIN)						
V_{EN_TH}	EN Threshold Voltage		-	2	-	V
SOFT-START						
T_{SS}	Internal soft-start time	10% to 90% of FB voltage	-	4	-	ms
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage	T_J = 25 °C	0.735	0.750	0.765	V
HIGH-SIDE MOSFET						
R_{DS_ON}	On-resistance	V_{IN} = 12 V, BOOT to SW = 5.8 V	-	150	-	mΩ
HIGH-SIDE MOSFET CURRENT LIMIT						
I_{LIMT}	Current limit	V_{IN} = 12 V, T_A = 25 °C, Open Loop	3.80	4.75	5.70	A
THERMAL PERFORMANCE						
T_{SHDN}	Thermal shutdown threshold		-	150	-	℃
T_{HYS}	Hysteresis		-	12	-	

Switching Characteristics

Over the recommended operating junction temperature range of -40 °C to 125 °C (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{SW}	Switching frequency	R_T = 49.9 kΩ	400	500	600	kHz
T_{ON_MIN}	Minimum controllable on time	V_{IN} = 12 V, BOOT to SW = 5.8 V, I_{Load} =1 A	-	160	-	ns
D_{MAX}	Maximum duty cycle	f_{SW} = 500 kHz	-	90%	-	-

Typical Application Circuit

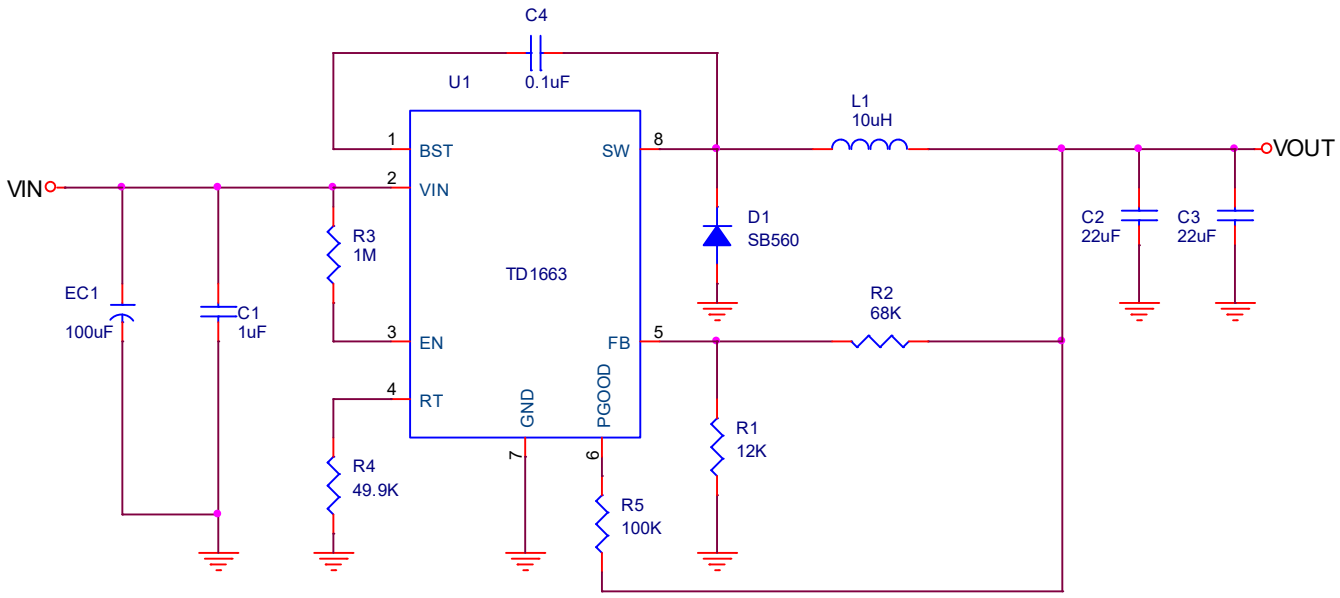
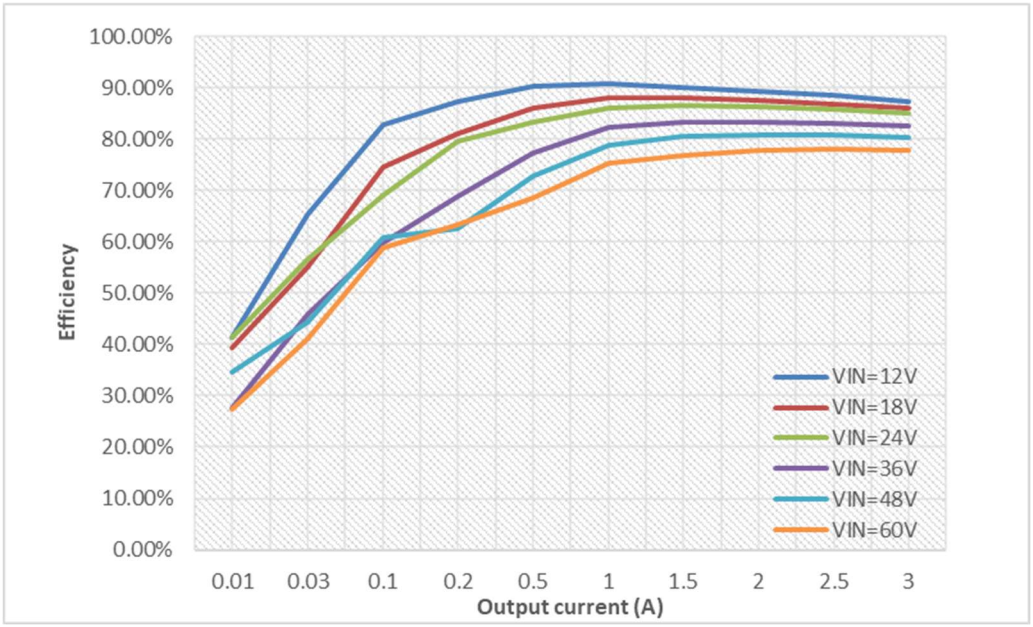


Figure2 Application Circuit, 5V Output



Efficiency @VOUT=5V，Fsw=500KHz

Function Description

Fixed Frequency Peak Current Mode Control

TD1663 output voltage is regulated by turning on the high-side N-MOSFET with controlled ON time. During high-side switch ON time, the SW pin voltage swings up to approximately VIN, and the inductor current i_L increase with linear slope ($V_{IN} – V_{OUT}$) / L. When high-side switch is off, inductor current discharges through freewheel diode with a slope of $–V_{OUT}$ / L. The control parameter of Buck converter is defined as Duty Cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal Buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

The TD1663 employs fixed frequency peak current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency at normal load condition. At very light load, the TD1663 will operate in Sleep-mode to maintain high efficiency and the switching frequency will decrease with reduced load current.

Slope Compensation

The TD1663 adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

Low Dropout Operation and Bootstrap Voltage (BOOT)

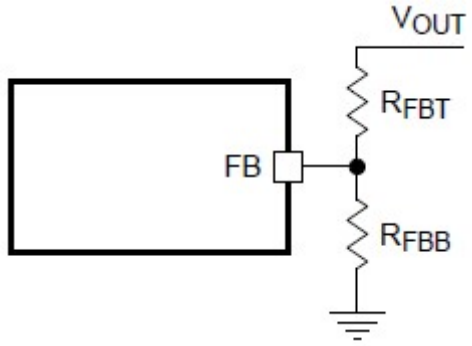
The TD1663 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the external low side diode conducts. The recommended value of the BOOT capacitor is 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16 V or greater is recommended for stable performance over temperature and voltage. When operating with a low voltage difference from input to output, the high-side MOSFET of the TD1663 will operate at approximate 95% duty cycle. When the voltage from BOOT to SW drops below 3.2 V, the high-side MOSFET is turned off and an integrated low side MOSFET pulls SW low to recharge the BOOT capacitor. Since the gate drive current sourced from the BOOT capacitor is small, the high-side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 95%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low side diode voltage and the printed circuit board resistance.

Adjustable Output Voltage

The internal voltage reference produces a precise 0.75 V (typical) voltage reference over the operating temperature range. The output voltage is set by a resistor divider from output voltage to the FB pin. It is recommended to use 1% tolerance or better and temperature coefficient of 100 ppm or less divider resistors. Select the low side resistor RFBB for the desired divider current and use Equation 1 to calculate high-side RFBT.

Larger value divider resistors are good for efficiency at light load. However, if the values are too high, the regulator will be more susceptible to noise and voltage errors from the FB input current may become noticeable. RFBB in the range from 10 kΩ

to 100 kΩ is recommended for most applications.



$$R_{FBT} = \frac{V_{OUT} - 0.75}{0.75} \times R_{FBB}$$

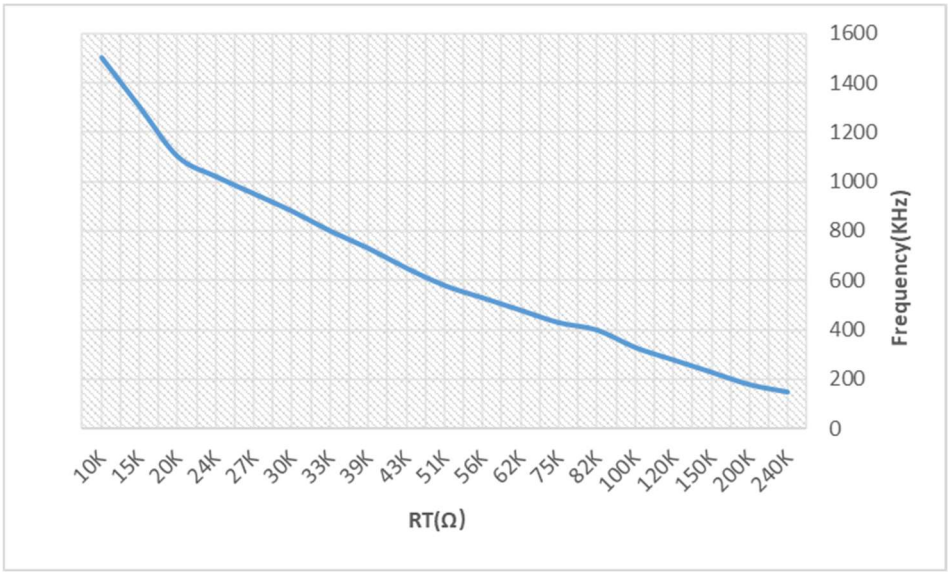
Enable and Adjustable Under-voltage Lockout

The TD1663 is enabled when the VIN pin voltage rises above 8.5 V (typical) and the EN pin voltage exceeds the enable threshold of 2 V (typical). The TD1663 is disabled when the VIN pin voltage falls below 7 V (typical) or when the EN pin voltage is below 2 V.

Switching Frequency and Synchronization (RT/SYNC)

The switching frequency of the TD1663 can be programmed by the resistor RT from the RT pin and GND pin. The RT pin can't be left floating or shorted to ground. To determine the timing resistance for a given switching frequency(200kHz-1MHz), use the below Equation:

$$R_T(k\Omega) = 42904 \times f_{SW}(kHz)^{-1.088}$$



RT(Ω)	Freq(KHz)
240K	150
200K	180
150K	230
120K	280
100K	330
82K	400
75K	430
62K	480
56K	530
51K	580
43K	650
39K	730
33K	800
30K	880
27K	950
24K	1020
20K	1100
15K	1300
10K	1500

Power Good (PGOOD)

The TD1663 has a built in power-good flag shown on PGOOD pin to indicate whether the output voltage is within its regulation level. The PGOOD signal can be used for start-up sequencing of multiple rails or fault protection. The PGOOD pin is an open-drain output that requires a pull-up resistor to an appropriate DC voltage. Voltage seen by the PGOOD pin should never exceed 7V. A resistor divider pair can be used to divide the voltage down from a higher potential. A typical range of pull-up resistor value is 10kΩ to 100kΩ.

When the FB voltage is within the power-good band, +7% above and -6% below the internal reference V_{REF} typically, the PGOOD switch will be turned off and the PGOOD voltage will be pulled up to the voltage level defined by the pull-up resistor or divider. When the FB voltage is outside of the tolerance band, +9% above or -8% below V_{REF} typically, the PGOOD switch will be turned on and the PGOOD pin voltage will be pulled low to indicate power bad.

Inductor

The inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will in turn result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining inductance is to allow the peak-to-peak ripple current to be about 40% of the output load current. Also, make sure that the peak inductor current is below the maximum switch current limit.

The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Where V_{OUT} is the output voltage, VIN is the input voltage, fs is the switching frequency, and ΔIL is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

$$I_P = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

where I_{LOAD} is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors. Since the input capacitor (C1) absorbs the input switching current, it requires and adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})}$$

The worst-case condition occurs at VIN=2V_{OUT}, where I_{C1} = I_{LOAD}/2. For simplification, use an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitor, be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C_1 \times f_s} \times \frac{V_{OUT}}{V_{IN}} (1 - \frac{V_{OUT}}{V_{IN}})$$

where C1 is the input capacitance Value.

Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Under typical application conditions, a minimum ceramic capacitor value of 20μF is recommended on the output. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{Vout}{f_s \times L} \times \left(1 - \frac{Vout}{Vin}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where C2 is the output capacitance value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance which is the main cause for the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C2} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

When using tantalum or electrolytic capacitors. The ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The TD1663 can be optimized for a wide range of capacitance and ESR values.

Over Current and Short Circuit Protection

The TD1663 is protected from over current condition by cycle-by-cycle current limiting on the peak current of the high-side MOSFET. High-side MOSFET over-current protection is implemented by the nature of the Peak Current Mode control. The high-side switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. Please refer to Functional Block Diagram for more details. The peak current of high-side switch is limited by a clamped

maximum peak current threshold which is constant. So the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

The TD1663 also implements a frequency fold-back to protect the converter in severe over-current or short conditions. The frequency fold-back increases the off time by increasing the period of the switching cycle, so that it provides more time for the inductor current to ramp down and leads to a lower average inductor current. Lower frequency also means lower switching loss. Frequency fold-back reduces power dissipation and prevents overheating and potential damage to the device.

Overvoltage Protection

The TD1663 employs an output overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. The OVP feature minimizes output overshoot by turning off high-side switch immediately when FB voltage reaches to the rising OVP threshold which is nominally 109% of the internal voltage reference VREF. When the FB voltage drops below the falling OVP threshold which is nominally 107% of VREF, the high-side MOSFET resumes normal operation.

Thermal Shutdown

The TD1663 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 150°C (typical). The high-side MOSFET stops switching when thermal shundown activates. Once the die temperature falls below 130°C (typical), the device reinitiates the power up sequence controlled by the internal soft-start circuitry.

Shutdown Mode

The EN pin provides electrical ON and OFF control for the TD1663. When VEN is below 1.0 V, the device is in shutdown mode. The switching regulator is turned off and the quiescent current drops to 1.0μA typically. The TD1663 also employs under voltage lock out protection. If VIN voltage is below the UVLO level, the regulator will be turned off.

Light Load Operation

When the load current is lower than half of the peak-to-peak inductor current in CCM, the TD1663 will operate in DCM. At even lighter current loads, Sleep-mode is activated to maintain high efficiency operation by reducing switching and gate drive losses.

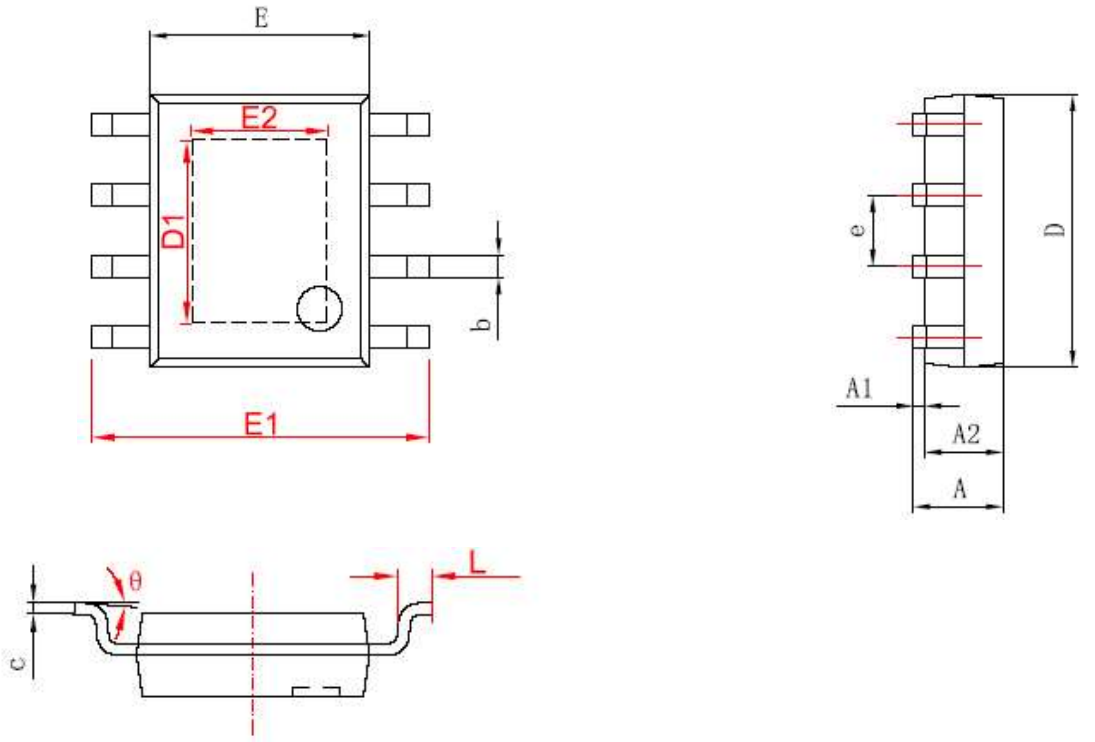
Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistor R_{FBT} and R_{FBB}, should be kept close to the FB pin. V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielding layer.
2. The input bypass capacitor C_{IN} must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD.
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor, C_{OUT} should be placed close to the junction of L and the diode D. The L, D, and C_{OUT} trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. The ground connection for the diode, C_{IN}, and C_{OUT} should be as small as possible and tied to the system ground plane in only one spot (preferably at the COUT ground point) to minimize conducted noise in the system ground plane.

Package Information

ESOP-8 Package Outline Dimensions



	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Design Notes