N-Channel Enhancement Mode MOSFET TDM2418A

DESCRIPTION

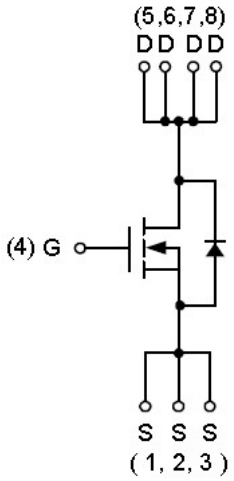
The TDM2418A uses advanced high cell density trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.

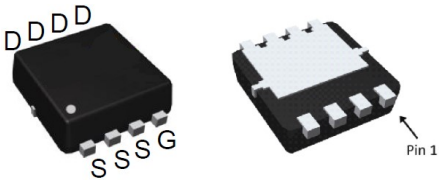
GENERAL FEATURES

- RDS(ON) < 6mΩ @ VGS=10V
  RDS(ON) < 8mΩ @ VGS=4.5V
- High Power and current handling capability
- Lead free product is available
- Surface Mount Package

Application

- Power Management in Desktop Computer or DC/DC Converters.





PPAK-3*3-8

ABSOLUTE MAXIMUM RATINGS(T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current @ Continuous(Note 5)	I_D（T_C=25℃）	55	A
	I_D（T_C=100℃）	34	A
Drain Current @ Current-Pulsed (Note 3)	I_{DM}（T_C=25℃）	220	A
Maximum Power Dissipation(Note 2)	P_D（T_C=25℃）	32	W
Avalanche Current, Single pulse (Note3,6)	I_{AS}(L=0.5mH)	19	A
Avalanche Energy, Single pulse (Note3,6)	E_{AS}(L=0.5mH)	90	mJ
Thermal Resistance-Junction to Case	$R_{\theta JC}$(Steady State)	3.95	°C/W
Thermal Resistance-Junction to Ambient(Note1,4)	$R_{\theta JA}$(Steady State)	62	°C/W
Operating Junction Temperature Range	T_J	-55 To 150	℃
Storage Temperature Range	T_{STG}	-55 To 150	℃

ELECTRICAL CHARACTERISTICS (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.2	1.7	2.5	V
Drain-Source On-State Resistance (Note4)	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A	-	4.3	6	mΩ
		V_{GS}=4.5V, I_D=10A	-	6.7	8	mΩ
Gate Resistance	R_g	V_{DS} = V_{GS}=0V, f = 1.0MHz	-	2.1	-	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, F=1.0MHz	-	972	-	PF
Output Capacitance	C_{oss}		-	725	-	PF
Reverse Transfer Capacitance	C_{rss}		-	64	-	PF
SWITCHING CHARACTERISTICS						
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=20V, V_{GS}=10V, R_G=1.6Ω, I_D=10A	-	5.8	-	nS
Turn-on Rise Time	t_r		-	7.3	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	28	-	nS
Turn-Off Fall Time	t_f		-	4.8	-	nS
Total Gate Charge	Q_g	V_{DS}=32V, I_D=10A, V_{GS}=10V	-	27.7	-	nC
Gate-Source Charge	Q_{gs}		-	5.6	-	nC
Gate-Drain Charge	Q_{gd}		-	3.8	-	nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 4)	V_{SD}	V_{GS}=0V, I_S=20A	-	0.85	1.1	V
Continuous Source Current	I_S		-	-	55	A
Body Diode Reverse Recovery Time	Trr	I_F=20A, dI/dt=100A/μs	-	20	-	nS
Body Diode Reverse Recovery Charge	Qrr		-	48	-	nC

Note 1：The value of $R\theta_{JC}$ is measured in a still air environment with T_A =25°C and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

Note 2：The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

Note 3. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

Note 4. The $R\theta_{JA}$ is the sum of the thermal impedance from junction to case $R\theta_{JC}$ and case to ambient.

Note 5. The maximum current rating is package limited.

Note 6. The EAS data shows Max. rating. The test condition is V_{DS}=32V, V_{GS}=10V, L=0.5mH

Typical Operating Characteristics

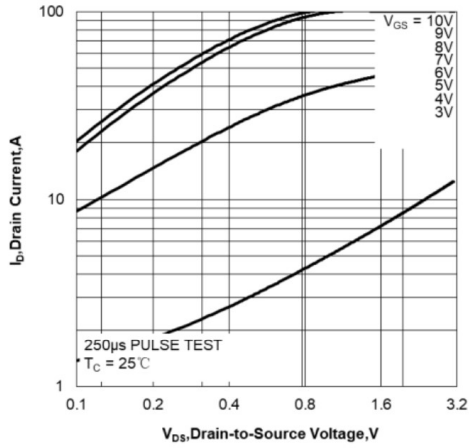


Figure 1. Output Characteristics

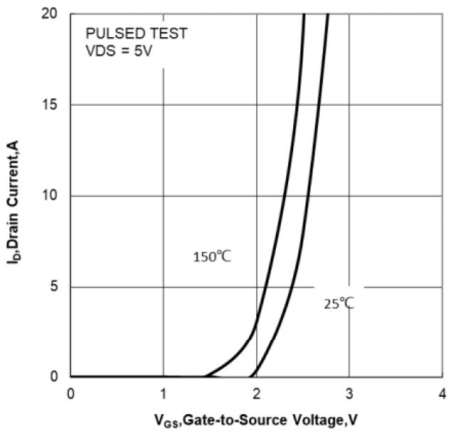


Figure 2. Transfer Characteristics

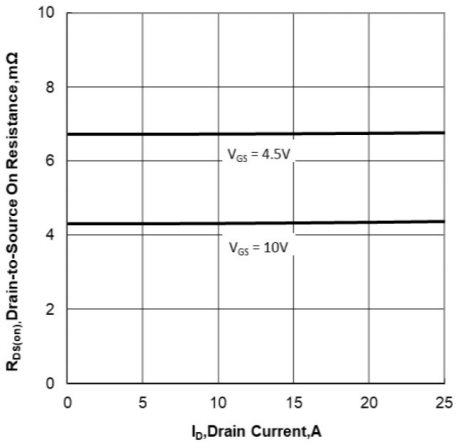


Figure 3. Drain-to-Source On Resistance vs Drain Current

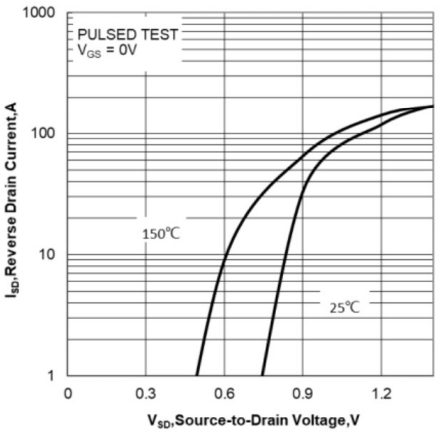


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

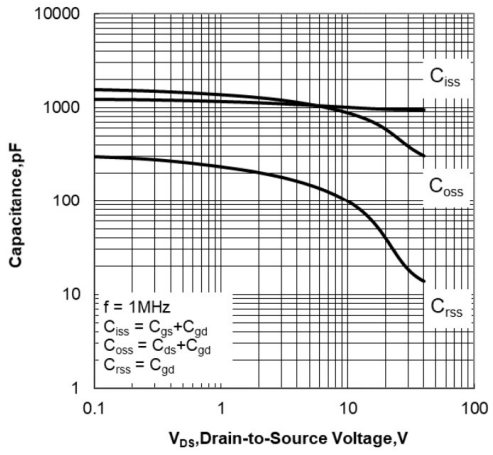


Figure 5. Capacitance Characteristics

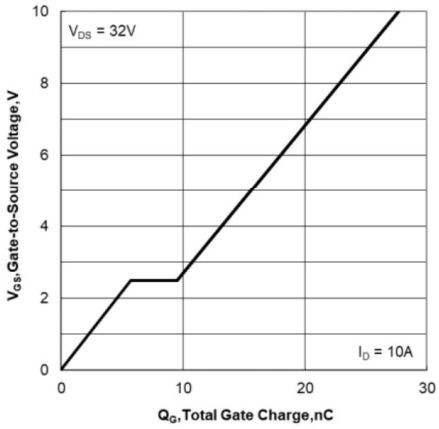


Figure 6. Gate Charge Characteristics

Typical Operating Characteristics(Cont.)

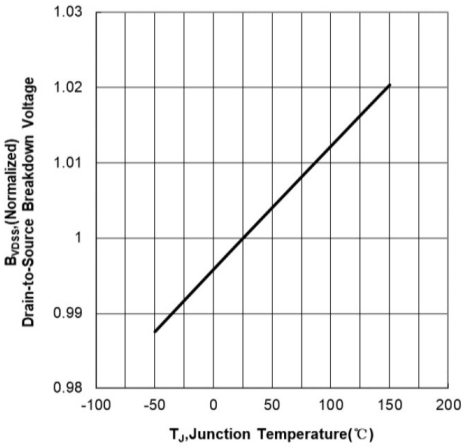


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

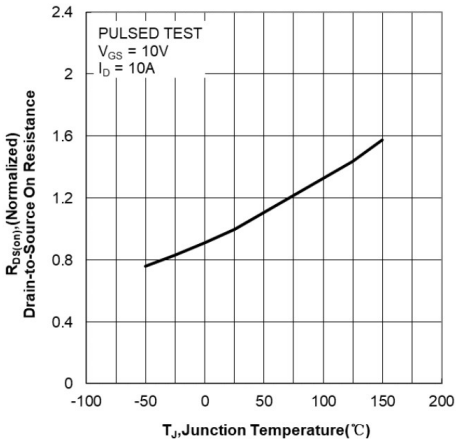


Figure 8. Normalized On Resistance vs Junction Temperature

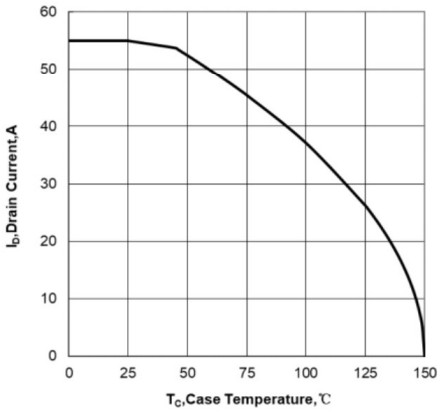


Figure 9. Maximum Continuous Drain Current vs Case Temperature

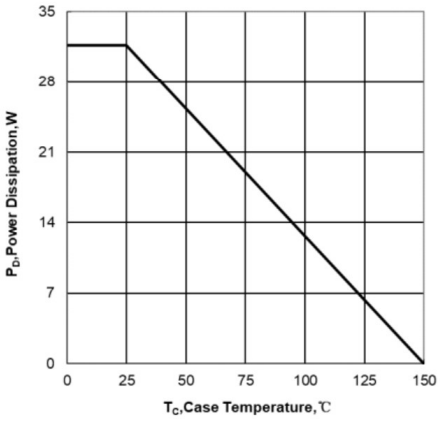


Figure 10. Maximum Power Dissipation vs Case Temperature

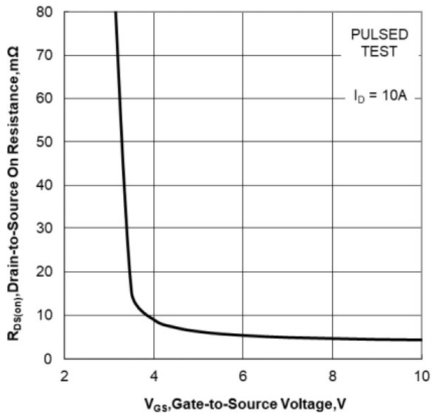


Figure 11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

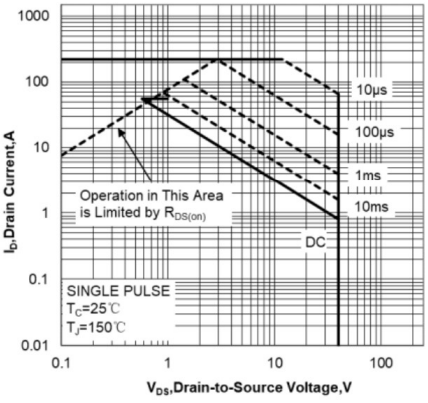


Figure 12. Maximum Safe Operating Area

Typical Operating Characteristics (Cont.)

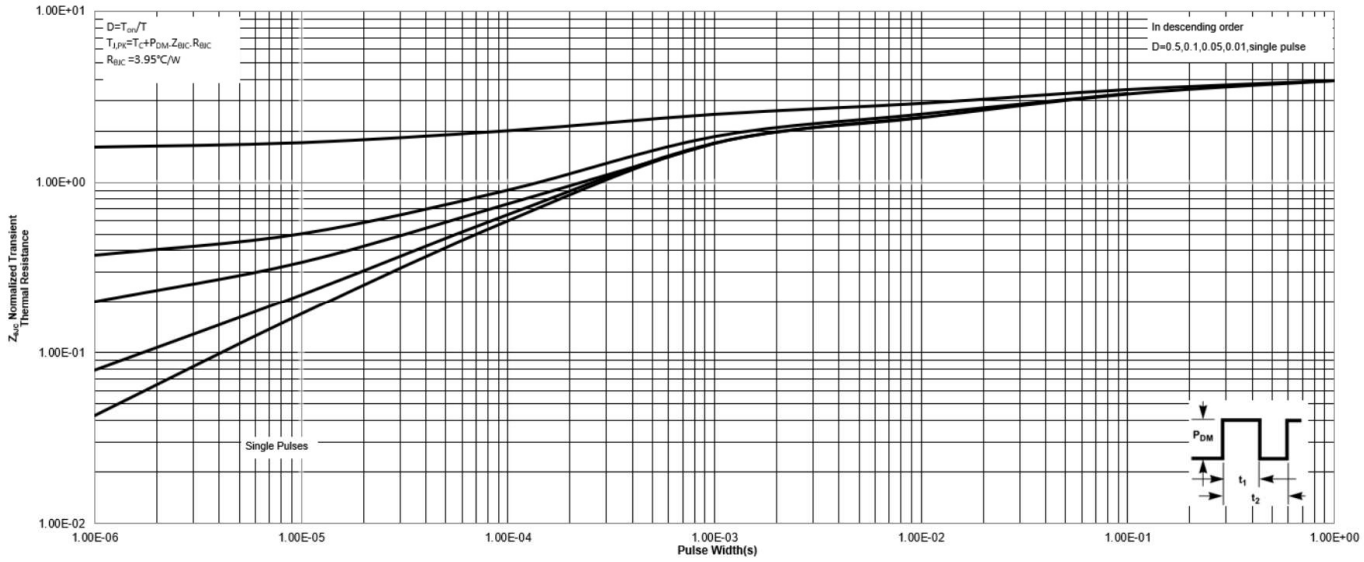
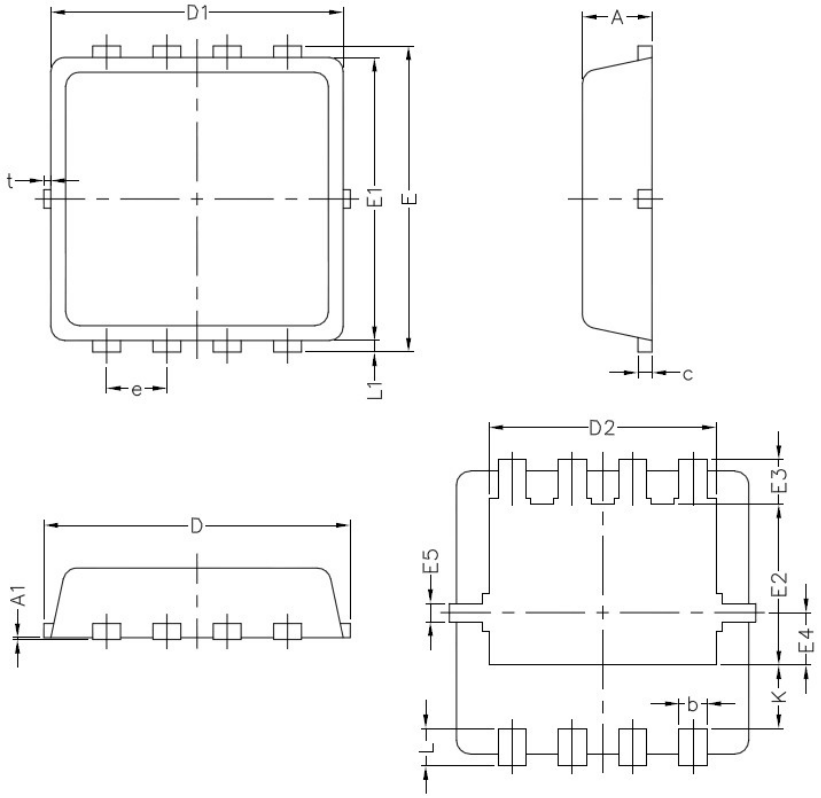


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Information

PPAK-3*3-8 Package



Symbol	PPAK-3*3-8(mm)		
	Min	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.3	3.45
D1	3.00	3.15	3.30
D2	2.25	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.68
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.49	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	/	/	0.13

Design Notes