

General Description

The TD1751 is a constant-on-time, synchronous, very compact PWM controller, which drives N-channel MOSFETs. The TD1751 provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the TD1751 provides very high efficiency over light to heavy loads with loading modulated switching frequencies. In PWM Mode, the converter works nearly at constant frequency for low-noise requirements.

The TD1751 is equipped with accurate positive current-limit, output under-voltage, and output over-voltage protections. The TD1751 has a 2ms digital soft-start and built-in an integrated output discharge method for soft-stop. An internal integrated soft-start ramps up the output voltage with programmable slew rate to reduce the start-up current. A soft-stop function actively discharges the output capacitors with controlled reverse inductor current.

The TD1751 is available in 16pin QFN3x3 package.

Features

- Operates Wide Input Voltage from 4.5V to 40V
- Adjustable Output Voltage from 0.8V to $V_{in} \times 98\%$
- Excellent Line and Load Transient Responses
- PFM Mode for Increased Light Load Efficiency
- Integrated MOSFET Drivers
- Adjustable Current-Limit Protection
- Over-Temperature Protection
- Switching Frequency: $125\text{kHz} \pm 25\text{kHz}$
- QFN3x3-16L Package
- Lead Free and Green Devices Available (RoHS Compliant)

Pin Configurations

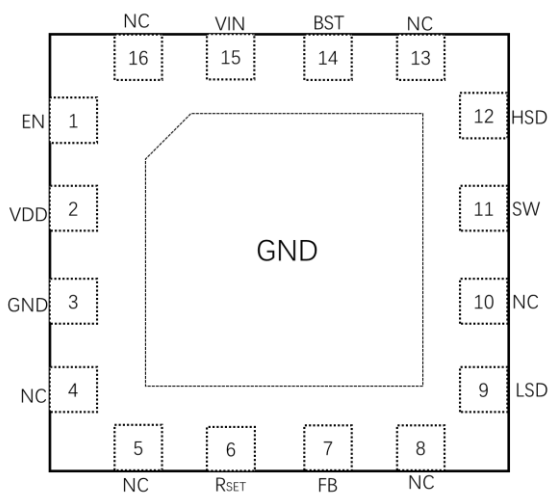


Figure1 Pin Configuration(Top View)

Applications

- PD Fast-Charge
- Cable Modems, Set Top Boxes and DSL Modems
- Industrial Power Supplies
- General-Purpose DC/DC Controller

Pin Description

Pin Number	Pin Name	Description
1	EN	Enable Input, Internal Pull-up.
2	VDD	Internal LDO Output.
3	GND	Ground.
4,5,8,10,13,16	NC	Not Connected.
6	R _{SET}	Over Current Setting.
7	FB	Feedback Of Output Voltage.
9	LSD	Low Side Driver Output.
11	SW	Switching Output, Connected with an Inductor.
12	HSD	High Side Driver Output.
14	BST	Boost-Strap.
15	VIN	Power Input.
	EPAD(GND)	Ground

Functional Block Diagram

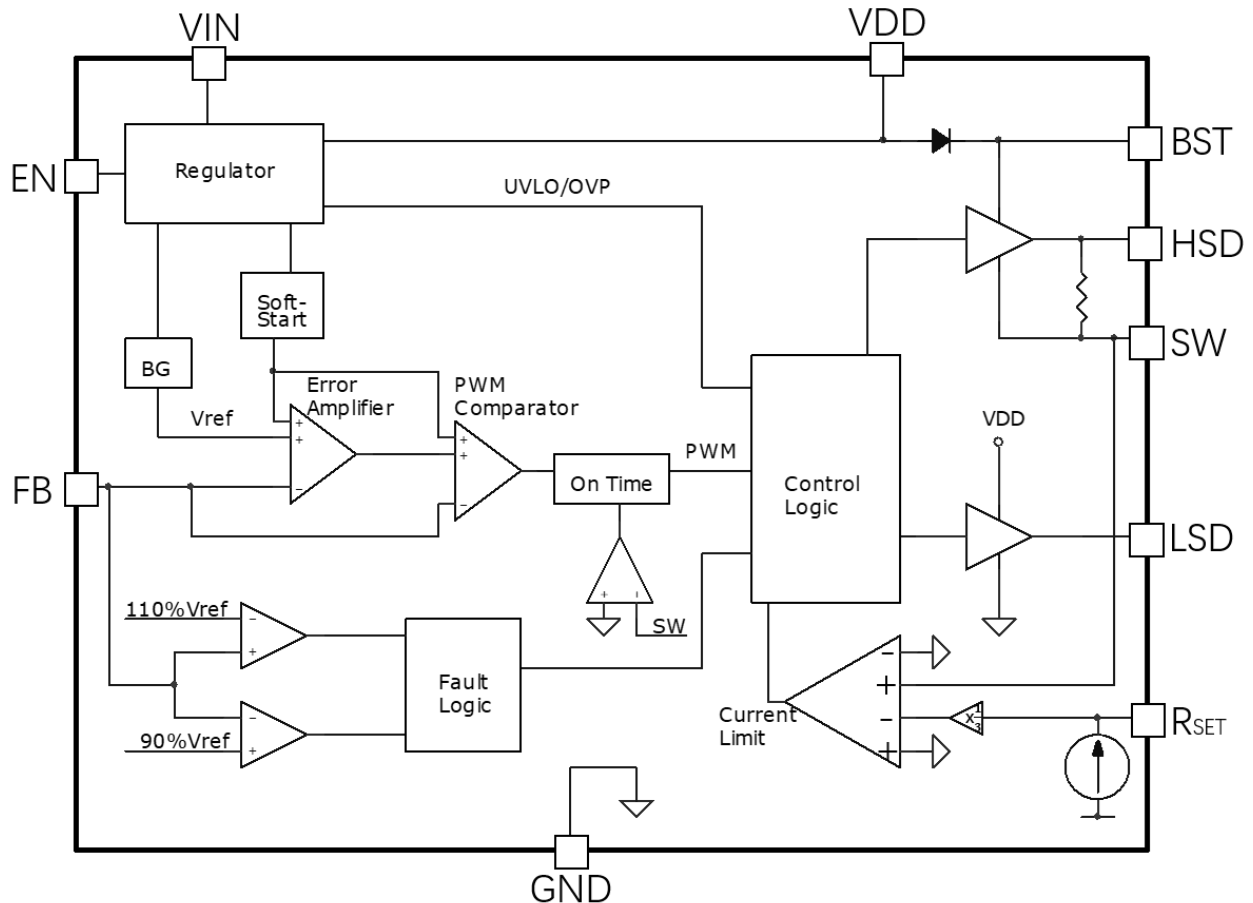


Figure 2 Functional Block Diagram

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
	VIN to GND	-0.3 to +43	V
	EN to GND	-0.3 to +43	V
	BST to GND	-0.3 to VIN+6	V
	SW to GND	-0.3 to VIN+0.6	V
	HSD to GND	-0.3 to V _{SW} +6	V
	VDD,FB,R _{SET} ,LSD to GND	-0.3 to +7	V
ESD	HBM (Human Body Mode)	2K	V
θ _{JA}	Thermal Resistance From Junction to Ambient	40	°C/W

Recommended Operating Conditions

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
V _{IN}	Supply Voltage	4.5	-	40	V
V _{OUT}	Output voltage range	0.8	-	V _{in} *98%	V
I _{OUT}	Output current range	-	-	15	A
T _A	Ambient Temperature	-40	-	85	°C
T _J	Junction Temperature	-40	-	125	°C

Electrical Characteristics

V_{IN}=12V, T_A=25°C, EN=12V (unless otherwise noted).

Symbol	Characteristic	Test conditions	Min.	Typ.	Max.	Unit
V _{IN}	Supply Voltage		4.5	-	40	V
I _{Q_VIN}	VIN Shutdown Current	EN=0V, VIN=12V	-	11	-	μA
	VIN Supply Current	No Switching, FB=1V	-	650	-	μA
VIN UVLO						
V _{UP}	VIN UVLO Turn ON	VIN Rising		4.3	4.4	V
V _{HYS}	VIN UVLO Hysteresis		-	400	-	mV
EN Voltage Threshold						
V _{EN_R}	EN Threshold, Rising		-	1.3	-	V
V _{EN_F}	EN Threshold, Falling		-	1.2	-	V
Feedback Voltage						
V _{FB}	Feedback voltage		0.784	0.800	0.816	V
	Tolerance		-2	-	2	%
Soft Start						
	Soft Start time		-	2	-	ms
Oscillator						
F _{SW}	Switch frequency		100	125	150	kHz
T _{ON}	Minimum On-Time		-	150	-	ns
D _{MAX}	Maximum Duty cycle		-	-	98	%
Current Sense						
V _{OCP}	Built-in Maximum OCP Voltage		110	-	-	mV
I _{OCSET}	OCSET Current Source		9	11	13	μA
	Over Current-limit Offset		-10	0	10	mV

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HSD & LSD Drivers

T _{RH}	HSD Rising Time		-	30	-	ns
T _{FH}	HSD Falling Time		-	20	-	ns
T _{RL}	LSD Rising Time		-	30	-	ns
T _{FL}	LSD Falling Time		-	20	-	ns
T _{LH}	Dead Time		-	30	-	ns
T _{HL}	Dead Time		-	30	-	ns

Thermal Shutdown (OTP)

T _{SD}	Temperature Rising		-	150	-	°C
T _{HYS}	OTP Hysteresis		-	20	-	°C

Typical Application Circuit

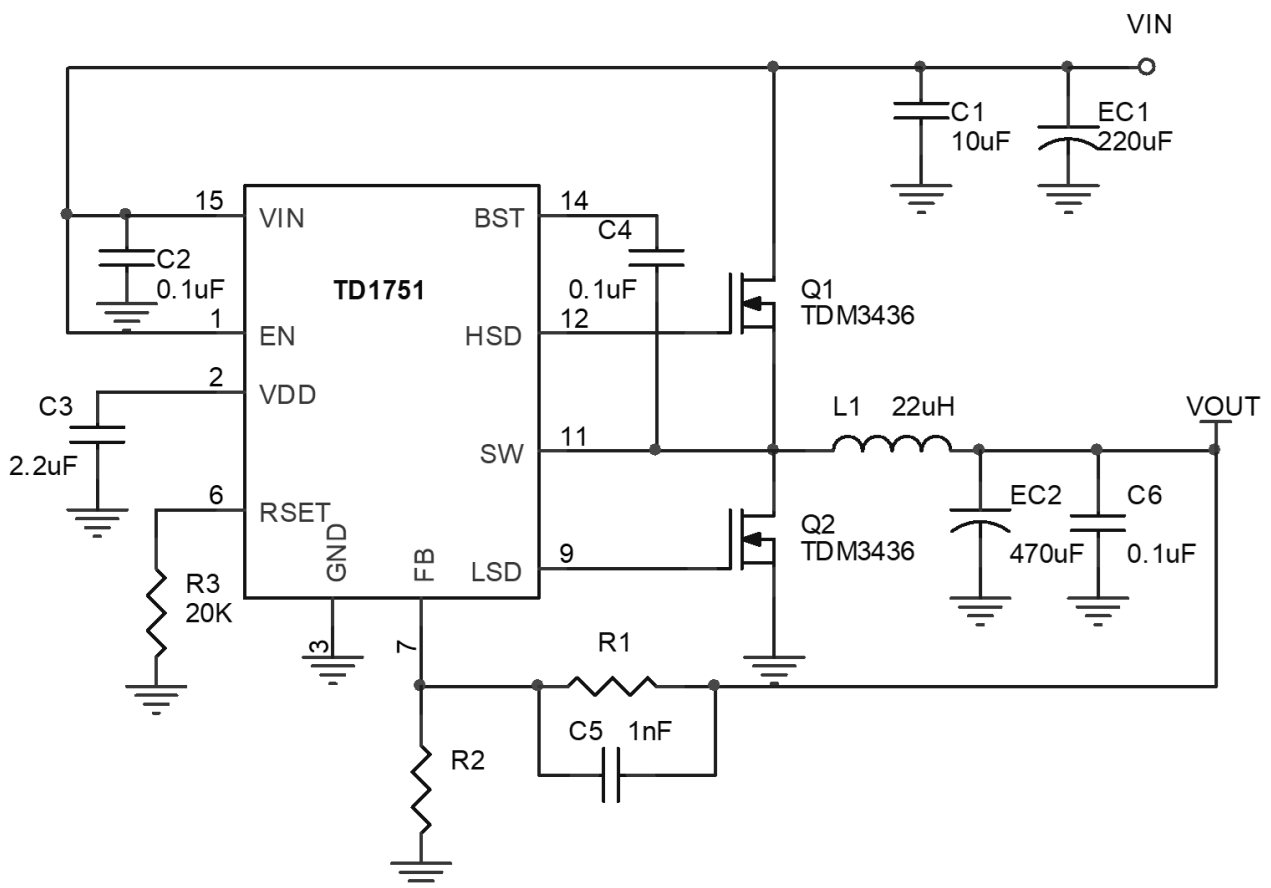


Figure 3 Typical Application

Function Description

The TD1751 is a fully integrated synchronous Buck controller employing constant on-time (COT) control scheme to achieve superior transient performance. Its proprietary internal ramp compensation offers stable operation with lower ESR ceramic output capacitors without using external complex compensation networks.

CONSTANT ON-TIME CONTROL

The constant on-time control (COT) operates by comparing the feedback voltage V_{FB} with the reference voltage (V_{FB}). When FB droops below the reference, the control circuit turns on HS switch immediately for a pre-determined period of time (on-time) to ramp up the inductor current. When this on-time times out, the LS switch is then turned on to ramp down the inductor current. The LS switch is turned off when inductor current reaches zero I_{ZX} (or triggers negative current limit I_{NEG} TD1751) or HS switch is turned on again for the next cycle. This operation repeats itself if FB droops below reference again.

The TD1751 uses a proprietary algorithm to calculate the on-time based on input voltage, output voltage and load current to achieve nearly constant switching frequency over entire continuous conduction load current range. The on-time can be estimated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} * 8\mu s$$

Due to its immediate response on FB voltage droop and simplified loop compensation, The TD1751 offers superior transient response compare to traditional fixed frequency PWM controller.

EN PIN CONTROL

The TD1751 is enable when the VIN pin voltage rises above 4.5V and the EN pin voltage exceeds the enable threshold of 1.3V. The TD1751 is disabled when the VIN pin voltage falls below 4V or when the EN pin voltage is below 1.2V. The EN pin has an internal pull-up current source that enables operation of the TD1751 when the EN pin floats.

RSET and CURRENT LIMIT

The over-current function protects the switching converter against over-current or short-circuit conditions. The controller senses the inductor current by detecting the drain-to-source voltage which is the product of the inductor's current and the on-resistance of the low-side MOSFET during its on-state. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor required.

A resistor (R_{SET}), connected from the R_{SET} to GND, programs the over-current trip level. Before the IC initiates a soft-start process, an internal current source, I_{OCSET} (11 μ A typical), flowing through the R_{SET} develops a voltage (V_{ROCSET}) across the R_{SET} . The device holds V_{ROCSET} and stops the current source, I_{OCSET} , during normal operation. When the voltage across the low-side MOSFET exceeds the $\frac{1}{3}V_{ROCSET}$, the controller turns off high-side MOSFET until the valley current reduce to the current limit below, then the high-side MOSFET will turn on again. The TD1751 has an internal OCP voltage, V_{OCP_MAX} , and the value is 0.11V typical. When the $R_{SET} * I_{OCSET} * \frac{1}{3}$ exceeds 0.11V or the R_{SET} is floating or not connected, the V_{ROCSET} will be the default value 0.11V. The over current threshold would be 0.11V across low-side MOSFET. The threshold of the valley inductor current limit is therefore given by:

$$I_{LIMIT} * R_{DS(ON)}(low-side) = \frac{1}{3} * I_{OCSET} * R_{SET}$$

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For the over-current is never occurred in the normal operating load range; the variation of all parameters in the above equation should be considered:

- The $R_{DS(ON)}$ of low-side MOSFET is varied by temperature and gate to source voltage. Users should determine the maximum $R_{DS(ON)}$ by using the manufacturer's datasheet.
- The minimum I_{OCSET} (9μA) and minimum R_{SET} should be used in the above equation.

Note that the I_{LIMIT} is the current flow through the low side MOSFET; I_{LIMIT} must be greater than valley inductor current which is output current minus the half of inductor ripple current.

$$I_{LIMIT} > I_{OUT(MAX)} - \frac{\Delta I}{2}$$

Where ΔI = output inductor ripple current

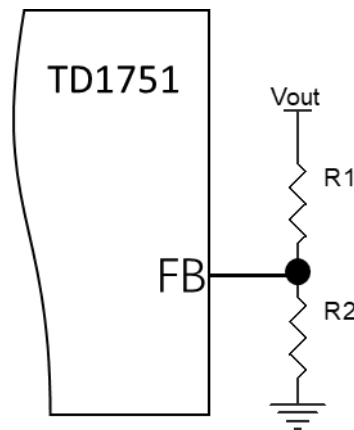
The overshoot and transient peak current also should be considered

Application Information

Output Voltage Setting

FB is the feedback pin and connected to the non-inverting of error amplifier input. The output voltage is adjustable from 0.8V to $V_{IN} \times 98\%$ with a resistor-divider connected with FB, GND and converter's output. Using 1% or better resistors for the resistor-divider is recommended.

The output voltage is determined by the equation:



$$V_{OUT} = 0.8 * (1 + \frac{R1}{R2})$$

Output Inductor Selection

The inductor value (L) determines the inductor ripple current, I_{RIPPLE} and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$L = \frac{V_{OUT}}{F_{SW} * I_{RIPPLE}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

F_{SW} : the switching frequency of the controller;

V_{IN}/V_{OUT} : input voltage/output voltage;

I_{RIPPLE} : the inductor ripple current and recommend $I_{RIPPLE} = 0.3 I_{OUT}$

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor which is capable of carrying the required peak current without going

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into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage. Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

Input Capacitor

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power-up, the input capacitors have to handle great amount of surge current. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low impedance PCB layout.

Output Capacitor

Output voltage ripple and the transient voltage deviation are factors which have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOS- FET turn-on and turnoff, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak inductor's current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8C_{OUT} * F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} * R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small de- coupling capacitor (1uF) in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered.

To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

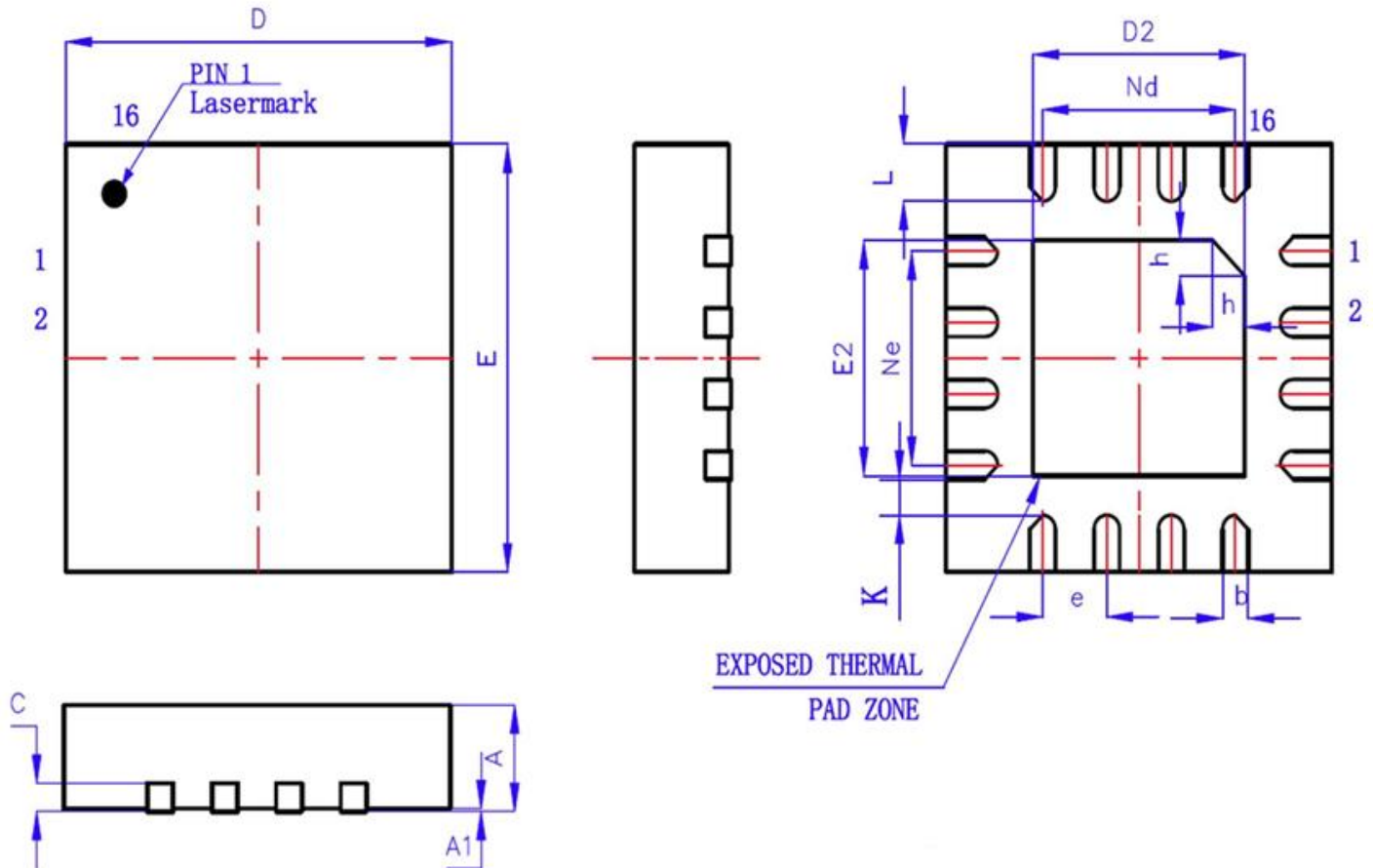
PCB Layout Considerations

For a controller, the layout is always an important step in design, A poor layout would result in poor performance, EMI problems, resistive loss and system instability. Following step would help to guarantee a good layout design:

- Keep the switching nodes (HSD, LSD, BST, and SW) away from sensitive small signal nodes. since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with these traces on any layer.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (V_{IN} and SW nodes) can get better heat sinking.
- The GND is the current sensing circuit reference ground and also the power ground of the LSD low-side MOSFET. On the other hand, the GND trace should be a separate trace and independently go to the source of the low-side MOSFET. Besides, the current sense resistor should be close to R_{SET} pin to avoid parasitic capacitor effect and noise coupling.
- Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible.)
- The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.
- Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces (HSD, LSD, BST, and SW).

Package Information

QFN16L Package Outline Dimensions



Symbol		A	A1	b	C	D	D2	e	Ne	Nd	E	E2	L	K	h
Milli meter	MIN	0.70	-	0.20	0.18	2.90	1.55	0.50 BSC	1.50 BSC	1.50 BSC	2.90	1.55	0.25	0.2	0.30
	NOM	0.75	0.02	0.25	0.20	3.00	1.65				3.00	1.65	0.30	-	0.35
	MAX	0.80	0.05	0.30	0.25	3.10	1.75				3.10	1.75	0.35	-	0.40

Application Notes