4 Inputs Selectable Stereo Class-AB Audio Amplifier TD9772A

General Description

TD9772A is an audio amplifier of Class-AB type. It offers both excellent sound quality of THD+N<0.03% , and input/output flexibilities. TD9772A features three different output configurations and four different input channels, both selectable by external pins. Outputs can be BTL,SE, or straight-through. There are four input channels making it convenient for the multigadgets modern age. On-chip DC volume control features 64 non-linear digital steps from –84dB to 24dB for better responsive to human ears While output power can be as high as 2.6W, the maximum output voltage can be adjusted by an external bias so that output power can be limited. Output pin short protection and over temperature shutdown modes are to ensure good system integrity. Internal soft switching designs are to minimize click and pop noises during power up/down, mute, and channel switching instances.

Features

◆ Vin: 2.5V to 5.5V
◆ Max Output Power (4-ohm speaker): 2.6W
- With 64 Steps Volume Control
- Adjustable max Output Power Limits
◆ 4 selectable Inputs
◆ Supports 3 Output configurations: BTL, SE, and Straight through.
- Maximum BTL gain: 24dB
- Maximum SE gain: 18dB
◆ Quiescent Current: <10mA
◆ Under Voltage Lockout at Vin <2V
◆ Short Circuit Protection
◆ Over Temperature Protection
◆ No Click and Pop noise: <10mW for BTL

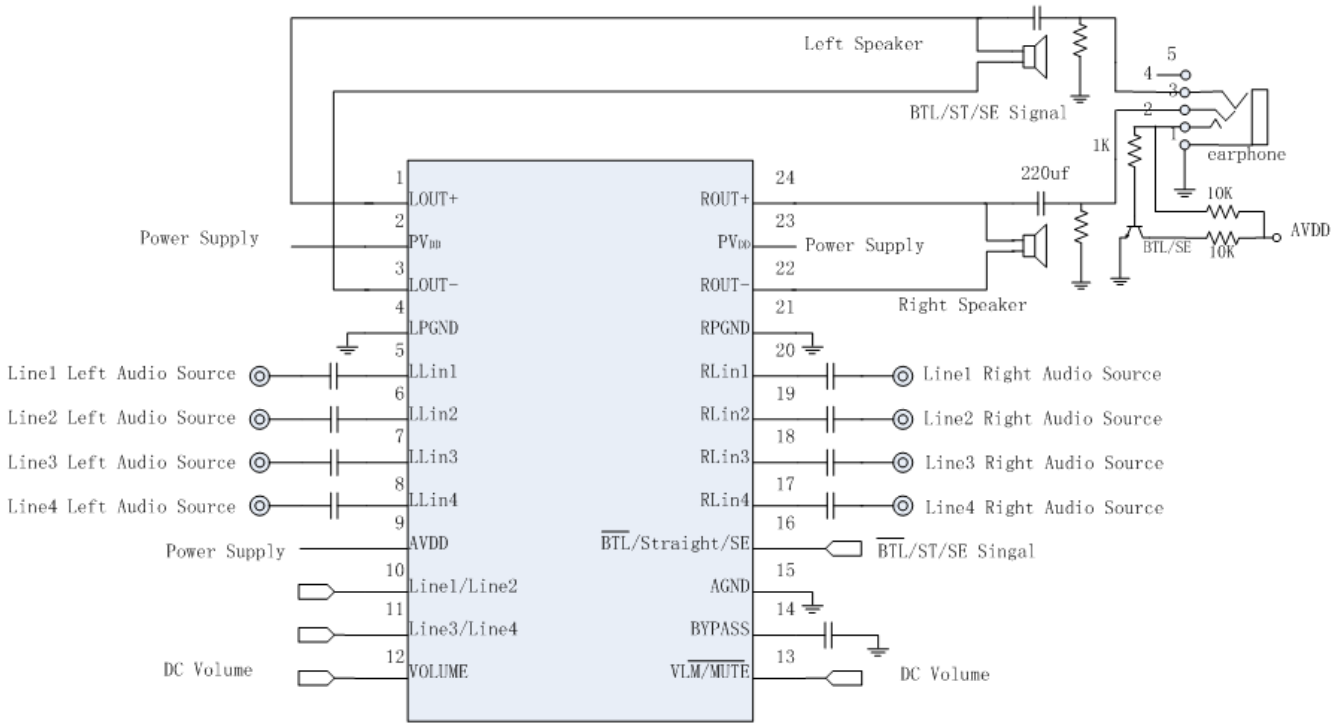
Applications

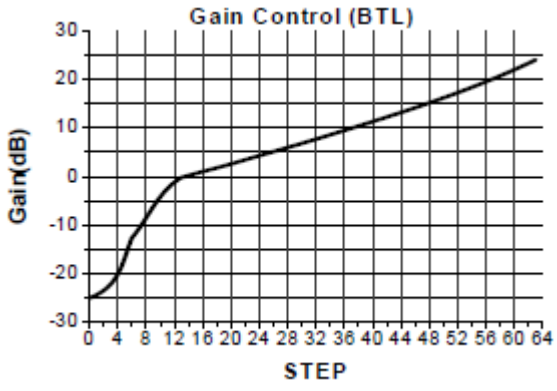
- Portable Music Center
- Notebook PC
- LCD Monitors

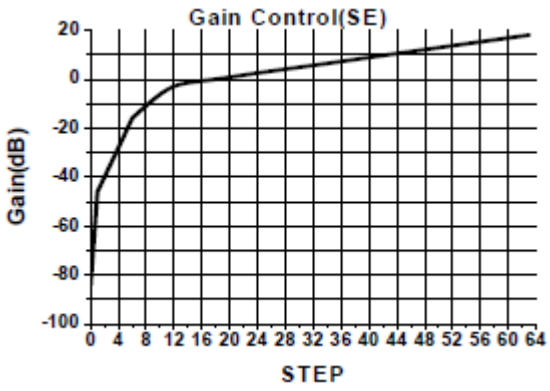
Ordering Information

Order Number	Package Type	Remark
	TSSOP-24L	

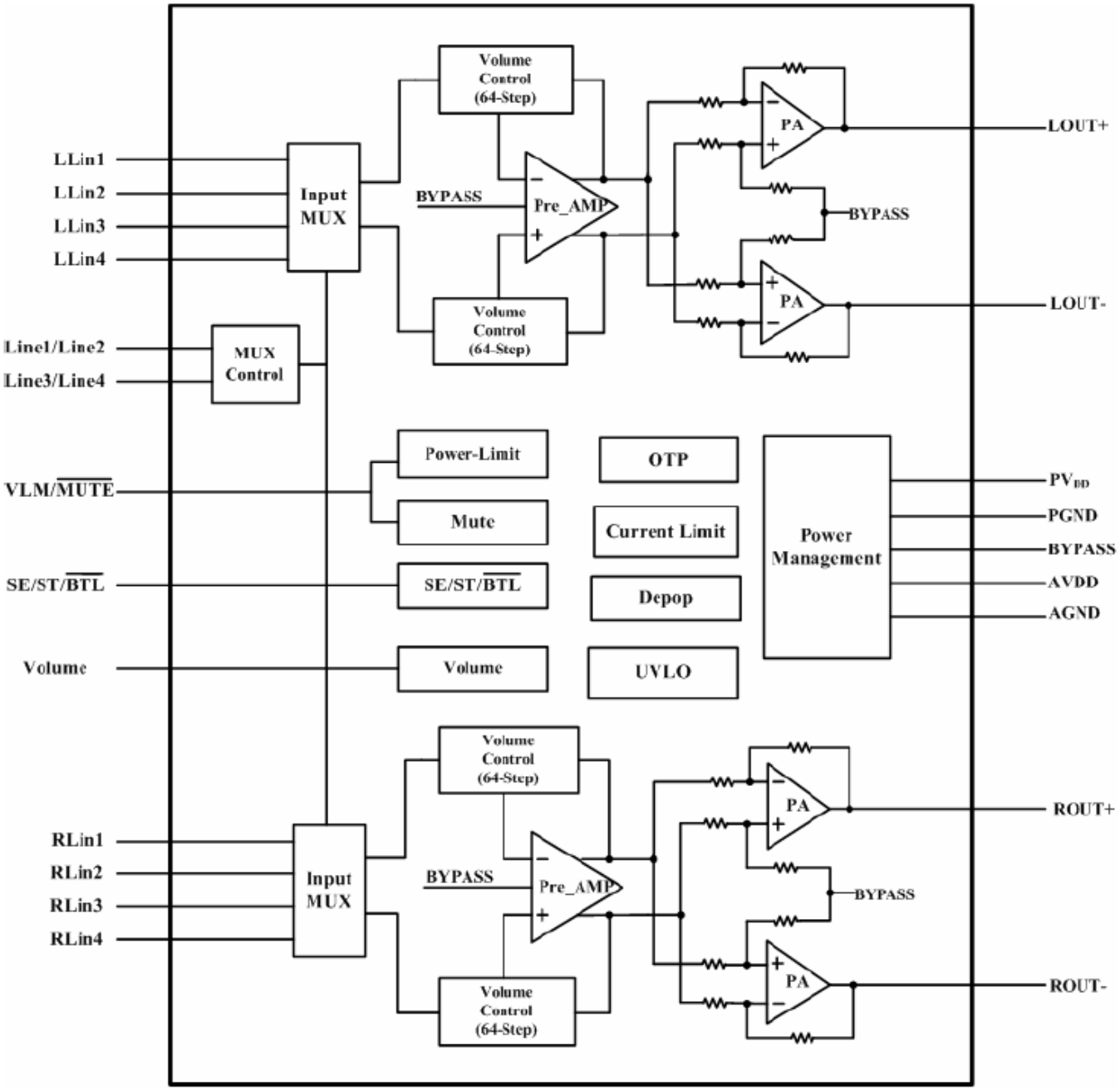
Typical Application Circuit



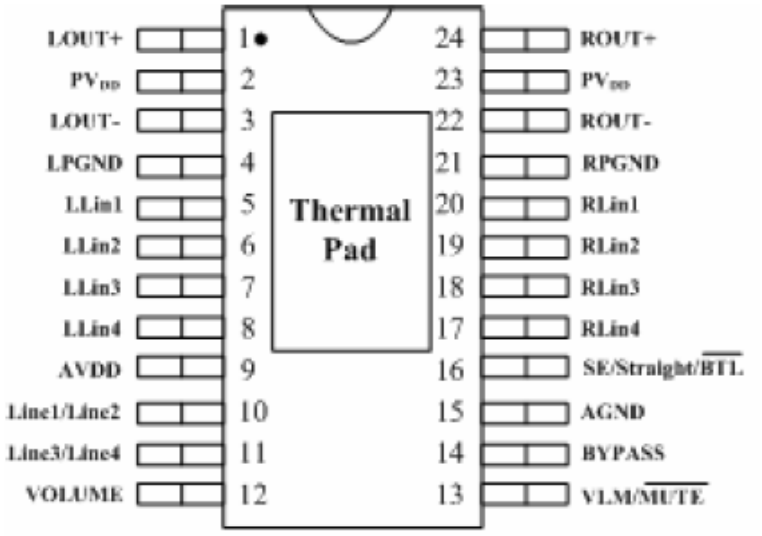




Functional Block Diagram



Pinout Configuration



Ordering Information

TD9772A □ □

Circuit Type

O:TSSOP-24

Packing:
Blank：Tube
R:Type and Reel

Pin Descriptions

SSOP-24 Pin		Description and Function
No.	**Pin Name**	
1, 24	LOUT+, ROUT+	Positive audio output terminals
2, 23	PV_{DD}	Supply voltage terminal for output power stage
3, 22	LOUT-, ROUT-	Negative audio output terminals
4, 21	LPGND, RPGND	Ground terminal for output power stage
5, 6 7, 8	LLin1, LLin2 LLin3, LLin4	Left channel line inputs
17, 18 19, 20	RLin1, RLin2 RLin3, RLin4	Right channel line inputs
9	AVDD	Supply voltage terminal for internal circuits
10, 11	Line1/Line2 Line3/Line4	Input MUX control (see Table 1 for selection logic)
12	VOLUME	Input voltage for setting volume gain (See Table 4 and graph)
13	VLM/MUTE	Input voltage for setting the maximum output voltage swing (See Table 3) ◆ 0V to VMute, Output driver is at tri-stated (Mute). ◆ Vlml to Vlmh, Output voltage is limited, see table 3. ◆ >Vlmh, Output voltage is at AVDD.
14	BYPASS	Connecting to a bypass cap of typical value 2.2uF.
15	AGND	Analog power supply ground
16	BTL/STRAIGHT/SE	Output mode selection (See Table 2 for selection logic) ◆ >VIL, output at BTL mode ◆ <VIH, output at SE mode ◆ Floating, output signal is the same as input signal

0: Logic input 0, VIL
1: Logic input 1, VIH N
C: No Connect

Table 1: Input Line Selection

Pin Line3/Line4	Pin Line1/Line2	Selection
0	0	Line1 inputs
0	1	Line2 inputs
1	0	Line3 inputs
1	1	Line4 inputs

Table 2: Output Mode Selection

BTL / Straight Through / $\overline{SE}$	Output Mode
0	BTL output
NC	Straight Through
1	SE out

Table 3: Output Voltage Limit

VLM / $\overline{Mute}$	Output Voltage
VMute	0(Mute State)
VLML < Vo < VLMH	AVDD/2-(VLM+0.6)<Vout<AVDD/2+(VLM+0.6)
> VLMH	0<Vout<AVDD

Table 4: Volume Control (For BTL Ouptput configuration)

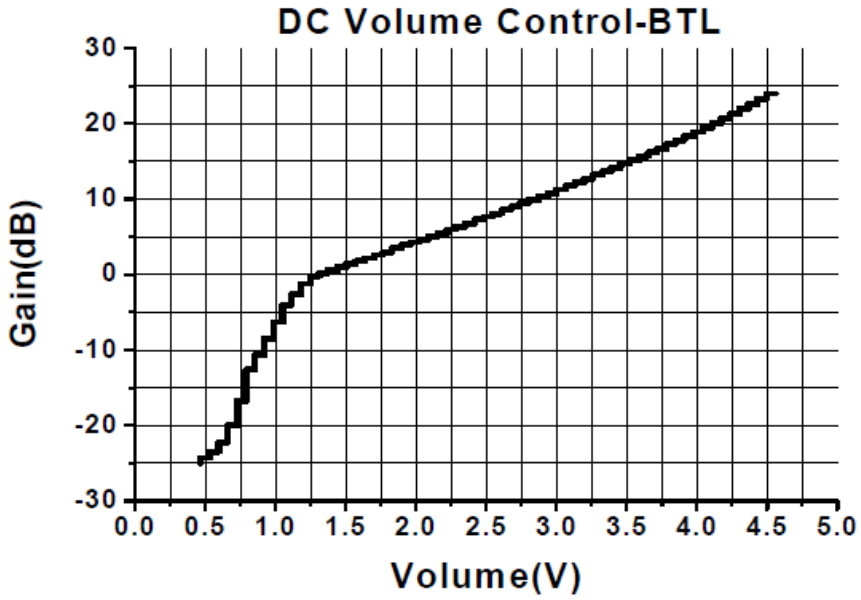


Table 5: Volume Control (For SE Ouptput configuration)

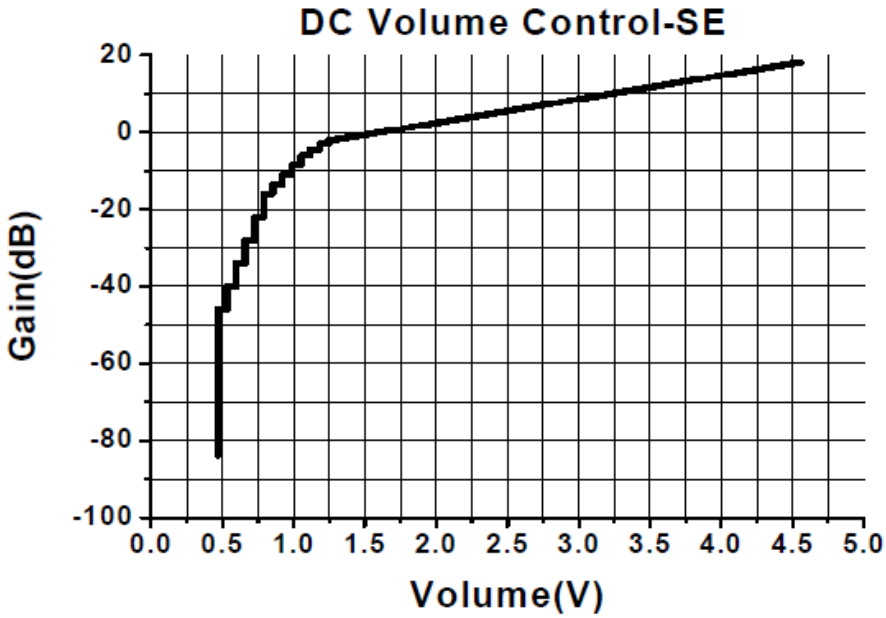


Table 6: DC Volume Control

STEP	Gain（dB）(SE)	Gain(dB) (BTL)	STEP	Gain（dB）(SE)	Gain(dB) (BTL)
0	-84	-25	32	5.6	7.7
1	-46	-24.3	33	6	8.1
2	-40	-23.5	34	6.4	8.6
3	-34	-22.2	35	6.8	9
4	-28	-20	36	7.2	9.5
5	-22	-16.8	37	7.6	9.9
6	-16	-12.6	38	8	10.4
7	-13.5	-10.7	39	8.4	10.8
8	-11	-8.5	40	8.8	11.3
9	-8.5	-6.3	41	9.2	11.8
10	-6	-4	42	9.6	12.2
11	-4.5	-2.6	43	10	12.7
12	-3	-1.2	44	10.4	13.2
13	-2	-0.2	45	10.8	13.7
14	-1.6	0.2	46	11.2	14.2
15	-1.2	0.6	47	11.6	14.7
16	-0.8	1	48	12	15.2
17	-0.4	1.4	49	12.4	15.7
18	0	1.8	50	12.8	16.2
19	0.4	2.2	51	13.2	16.7
20	0.8	2.6	52	13.6	17.3
21	1.2	3	53	14	17.8
22	1.6	3.5	54	14.4	18.4
23	2	3.9	55	14.8	18.9
24	2.4	4.3	56	15.2	19.5
25	2.8	4.7	57	15.6	20.1
26	3.2	5.1	58	16	20.7
27	3.6	5.5	59	16.4	21.3
28	4	6	60	16.8	22
29	4.4	6.4	61	17.2	22.6
30	4.8	6.8	62	17.6	23.3
31	5.2	7.3	63	18	24

Absolute Maximum Ratings

Supply voltage, AVDD, PV_{DD} ---------- 7.5V
Inputs ---------- -1.5V to V_{DD}+1.5V
(Line1/Line2, Line3/Line4, BTL/Straight/SE, Lin1-4, Volume, VLM/Mute, Bypass)

Recommended Operating Conditions

Supply voltage,AV_{DD},PV_{DD} ---------- 2.5V to 5.5V
Logic inputs ---------- -0.3V to AVDD+0.3V
(Line1/Line2, Line3/Line4, BTL/Straight/SE)
Signal inputs ---------- 0V to AVDD-1.0V
(Lin1 to Lin4, Volume, VLM/Mute)
Temperature (Ambient) ---------- -20C to 85C
Temperature (Junction) ---------- -20C to 125C

Electrical Characteristics

Operating Characteristics, BTL mode. V_{DD}=5V, T_A=25°C, RL=4Ω (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Voltage	V_{DD}		2.5		5.5	V
Quiescent Current	Iq	No Load SE/ST/BTL=0V	8	10	16	mA
		No Load SE/ST/BTL=5V	5	6.5	10	
Output Offset Voltage	Vos	No Load		1.1		mV
Under Voltage Lockout	UVLO				2	V
Maximum Output Power	P_O	THD=10%, R_L=3Ω, Fin=1kHz		2.9		W
		THD=10%, R_L=4Ω, Fin=1kHz		2.6		
		THD=10%, R_L=8Ω, Fin=1kHz		1.6		
		THD=1%, R_L=3Ω, Fin=1kHz		2.4		
		THD=1%, R_L=4Ω, Fin=1kHz		1.8		
		THD=0.5%, R_L=8Ω, Fin=1kHz	1	1.3		
Total Harmonic Distortion Plus Noise	THD+N	P_O=2.6W, R_L=4Ω, Fin=1kHz BTL		0.05		%
		P_O=75mW,R_L=32Ω, Fin=1kHz SE		0.02		
Power Ripple Rejection Ratio	PSRR	V_{IN}=0.1Vrms, R_L=8Ω, C_B=1μF, Fin=120Hz		60		dB
Drain-Source On-State Resistance	$R_{DS(ON)}$	IDS=1.6mA P MOSFET		144		mΩ
		IDS=1.6mA N MOSFET		147		
Input Crosstalk	IC	C_B=2.2uF, R_L=4Ω, f=1KHz		-40		dB

Electrical Characteristics(Cont.)

Operating Characteristics, BTL mode. V_{DD}=5V, T_A=25°C, RL=4Ω (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Oscillator Frequency	fosc		207	250	313	KHz
Efficiency	η	RL=4Ω , PO=2.6W, f=1KHz, BTL		71		%
Signal Noise Ratio	SNR	RL=4Ω , PO=2.6W, f=1KHz, BTL		97		dB
Input Logic Voltage	VIL				0.8	V
	VIH		2.0			V
Volume Input Range	Vol		0		AVDD-1.0	V
Mute Voltage	Vmute	Output Driver at tri-stated	0.5	0.6	0.7	V
Output Voltage Limit	VLML		0.7	0.8	0.9	V
	VLMH		1.8		2.0	V

Application Descriptions

Input Mux Operation

The TD9772A has 4 selectable inputs: Line1 input, Line2 input, Line3 input and Line4 input. The input MUX allows these four separate inputs to be applied to the amplifier. This allows the designer to choose which input is active independent of the state of the Line1/Line2 and Line3/Line4 terminals (see Table 1).

Output SE/Straght Through/BTL Operation

The ability of the TD9772A to easily switch between different output modes is one of its most important costs saving features. Internal to the TD9772A, three output states (BTL, Straight Through, SE) are designed. As shown in Table2 ,When the output pin is connected to a speaker, the pin BTL/Straight Through/SE is connected to a logic low voltage(<0.8V) and the output mode is selected as BTL mode. At the same time, the gain of the amplifier is the gain corresponding to BTL(see Table 4). Similarly, the SE output mode and SE gain (see Table 5) can be in effect when an earphone is inserted, at which time a logic high voltage (>AVDD-0.8V) is connected to the pin BTL/Straight Through/SE. The output is selected as ST(Straight Through) mode in other cases .

Mute and Power limit Operation

The VLM/MUTE pin is an input for controlling the mute and power-limit function of the TD9772A(see Table 3).When a logic low(<0.7V) is connected on this pin makes the chip in mute mode (Min Gain). When a limit voltage (0.7V~1.9V), the swing of output voltage is clamped between VPL (AVDD/2-(VLM+0.6V)) and VPH(AVDD/2+(VLM+0.6V)) . The output voltage is not be clamped and the chip is not be mute when the pin VLM/MUTE is connectedto a voltage, which is bigger than 2V.

Under Voltage Lock-out (UVLO)

The TD9772A incorporates circuitry designed to detect when the supply voltage is low. When the supply voltage drops to 1.8V or below, the TD9772A outputs are disabled, and the device comes out of this state and starts to normal functional once VDD≥2.0V.

Current Limit

The TD9772A has current limit circuitry on the outputs that prevents the device from being damaged when the outputto-output, output-to-VDD and output to GND short.When a short circuit is occuring, the max current of output is clamped in 2A.

Optimizing Depop Circuitry

Rapid on/off switching of the device will cause the click and pop noise. Circuitry has been included in the TD9772A to minimize the amount of popping noise when the chip is powered on.