

General Description

The TD8577 devices provide a power supply solution for products powered by either a one-cell Li-Ion or Li-polymer, or a two to three-cell alkaline, NiCd or NiMH battery. The converter generates a stable output voltage that is adjusted by an external resistor divider or fixed internally on the chip. It provides high efficient power conversion and is capable of delivering output currents up to 1 A at 5 V at a supply voltage down to 1.8 V. The implemented boost converter is based on a fixed frequency, pulse-width- modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency. At low load currents the converter enters Power Save mode to maintain a high efficiency over a wide load current range. The Power Save mode can be disabled, forcing the converter to operate at a fixed switching frequency. It can also operate synchronized to an external clock signal that is applied to the SYNC pin. the maximum peak current in the boost switch is limited to a value of 5000 mA.

The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. A low-EMI mode is implemented to reduce ringing and, in effect, lower radiated electromagnetic energy when the converter enters the discontinuous conduction mode. The device is packaged in a 16-pin QFN package measuring 4 mm x 4 mm (RSA) or in a 16-pin TSSOP16.or in a DFN3x3-12 packages

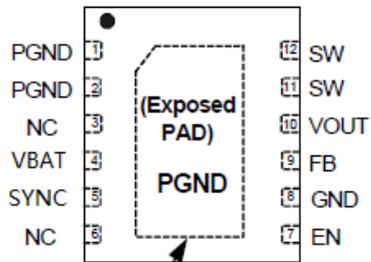
Features

- 92% Efficient Synchronous Boost Converter With 1000-mA Output Current From 1.8-V Input
- Device Quiescent Current: 20- μ A (Typ)
- Input Voltage Range: 1.8-V to 5.5-V
- Adjustable Output Voltage Options Up to 5.5-V
- Power Save Mode for Improved Efficiency at Low Output Power
- Low Battery Comparator
- Low EMI-Converter (Integrated Antiringing Switch)
- Load Disconnect During Shutdown
- Over-Temperature Protection
- Available in a Small 4 mm x 4 mm QFN-16 or in a TSSOP-16 or in a DFN3*3-12 package

Applications

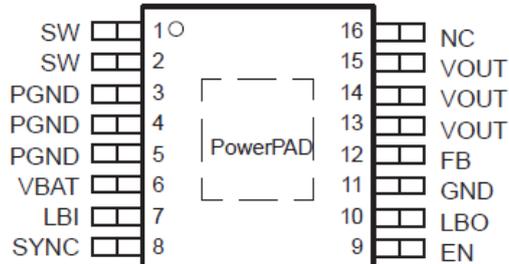
- Power Bank
- Tablet
- Portable Equipment

Pin Configurations

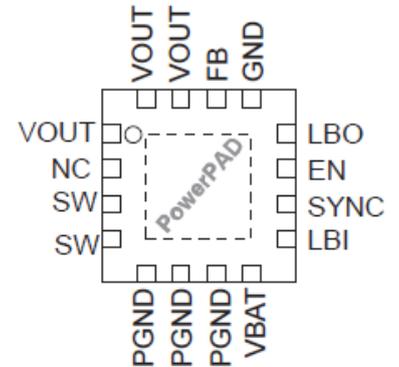


Exposed PAD on bankside

DFN3*3-12



TSSOP-16

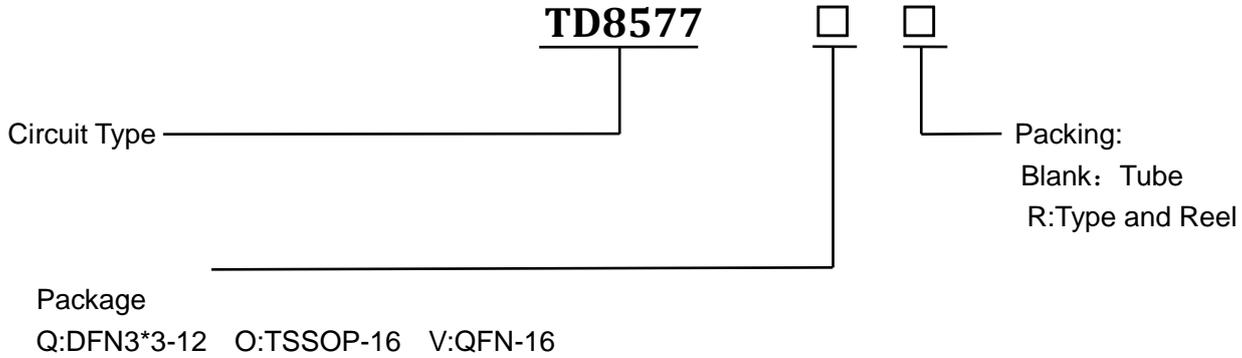


QFN-16

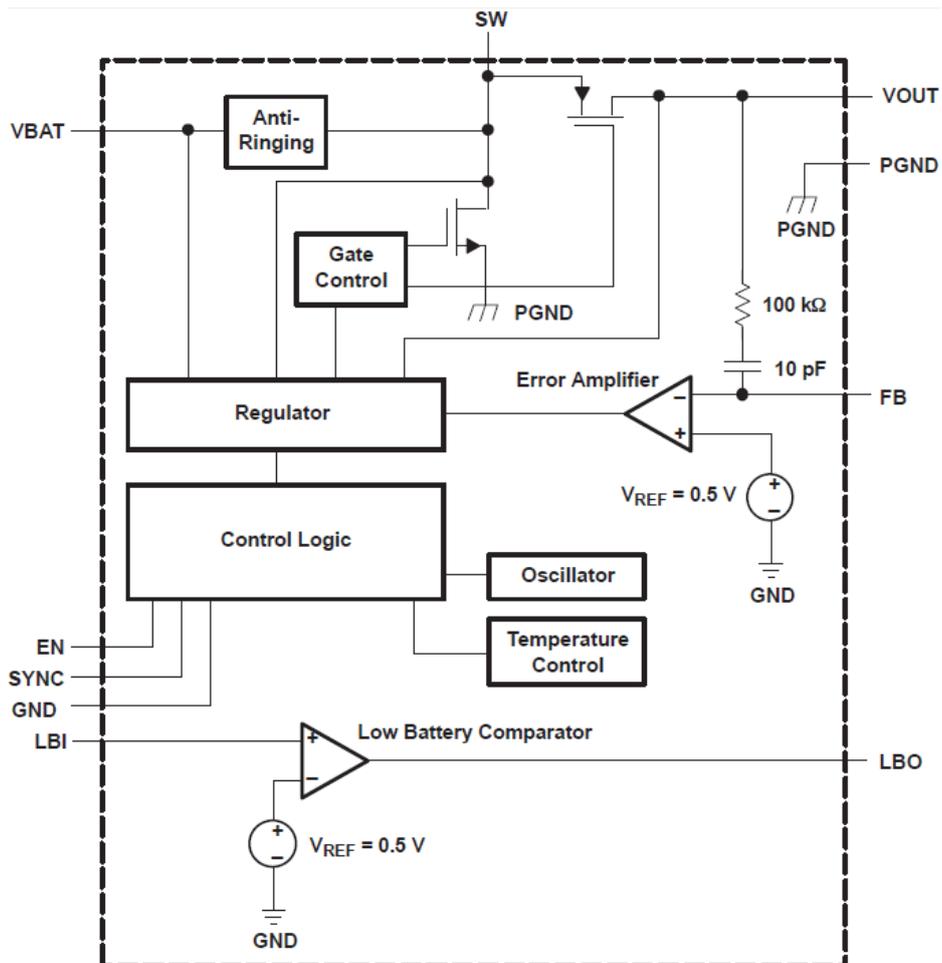
Pin Description

NO.			NAME	FUNCTION
DFN-12	TSSOP-16	QFN-16		
11,12	1,2	3,4	SW	Boost and rectifying switch input
1,2	3,4,5	5,6,7	PGND	Power ground
4	6	8	VBAT	Supply voltage
-	7	9	LBI	Low battery comparator input (comparator enabled with EN)
5	8	10	SYNC	Enable/disable power save mode (1/VBAT disabled, 0/GND enabled, clock signal for synchronization)
7	9	11	EN	Enable input. (1/VBAT enabled, 0/GND disabled)
-	10	12	LBO	Low battery comparator output (open drain)
8	11	13	GND	Control/logic ground
9	12	14	FB	Voltage feedback
10	13,14,15	1,15,16	VOUT	DC/DC output
3,6	16	2	NC	Not connected

Ordering Information



Functional Block Diagram



Absolute Maximum Ratings

Input voltage range on LBI	-0.3 V to 3.6 V
Input voltage range on SW, VOUT, LBO, VBAT, SYNC, EN, FB	-0.3 V to 7 V
Maximum junction temperature T _J	-40°C to 150°C
Storage temperature range T _{stg}	-65°C to 150°C

Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage at VBAT, V _I	1.8	5.5	V
Operating ambient temperature range, T _A	-40	85	°C
Operating virtual junction temperature range, T _J	-40	125	°C

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ _{JA}	Junction-to-Ambient Resistance in free air	TQFN4x4-16	40	°C/W
		DFN3x3-12	50	
		TSSOP-16	80	
θ _{JC}	Junction-to-Case Resistance	TQFN4x4-16	15	°C/W
		DFN3x3-12	20	
		TSSOP-16	20	

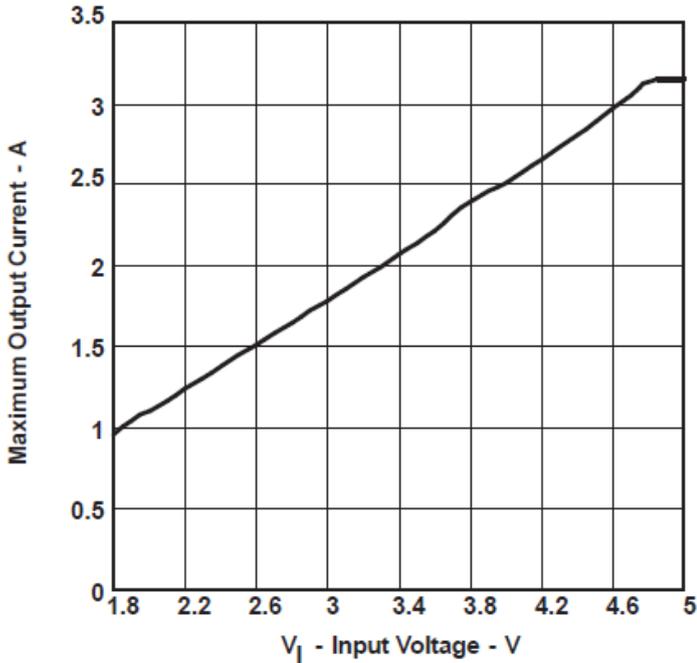
Note :is measured with the component mounted on a high effective thermal conductivity test board in free air.

Electrical Characteristics

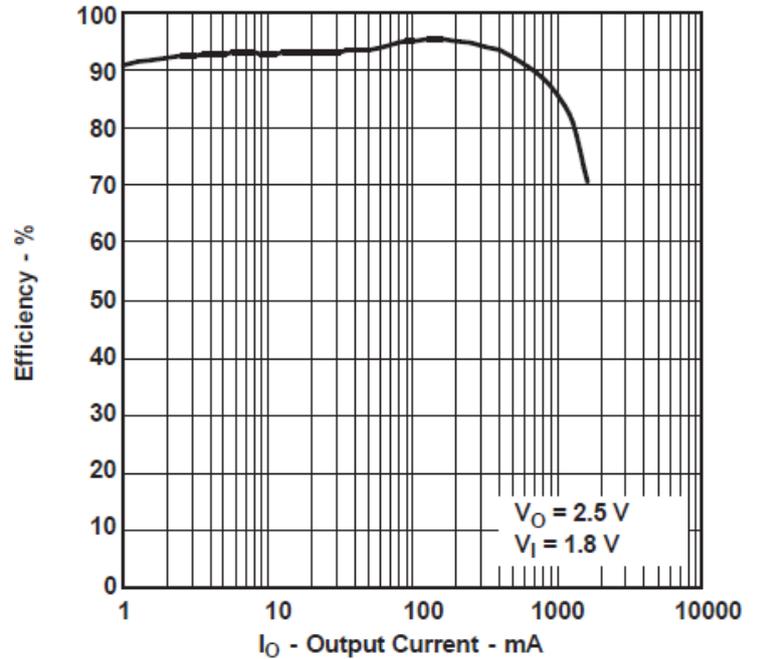
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vi Input voltage range			1.8		5.5	V
Vo TD8577 output voltage range			1.8		5.5	V
VFB TD8577 feedback voltage			490	500	510	mV
f Oscillator frequency			900	1200	1500	kHz
Frequency range for synchronization			900		1500	kHz
Switch current limit		VOUT = 5 V	4500	5000	5500	mA
Start-up current limit				0.4 x Isw		mA
SWN switch on resistance		VOUT = 5 V		55		mΩ
SWP switch on resistance		VOUT = 5 V		55		mΩ
Total accuracy			-3%		3%	
Line regulation					0.6%	
Load regulation					0.6%	
Quiescent current	VBAT	Io = 0 mA, VEN = VBAT = 1.8 V, VOUT = 5 V		10	25	μA
	VOUT	Io = 0 mA, VEN = VBAT = 1.8 V, VOUT = 5 V		10	20	μA
Shutdown current		VEN = 0 V, VBAT = 2.4 V		0.1	1	μA
CONTROL STAGE						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VUVLO	Under voltage lockout threshold	VLBI voltage decreasing		1.5		V
VIL	LBI voltage threshold	VLBI voltage decreasing	490	500	510	mV
	LBI input hysteresis			10		mV
	LBI input current	EN = VBAT or GND		0.01	0.1	μA
	LBO output low voltage	Vo = 3.3 V, Io = 100 μA		0.04	0.4	V
	LBO output low current			100		μA
	LBO output leakage current	VLBO = 7 V		0.01	0.1	μA
VIL	EN, SYNC input low voltage				0.2 x VBAT	V
VIH	EN, SYNC input high voltage		0.8 x VBAT			V
	EN, SYNC input current	Clamped on GND or VBAT		0.01	0.1	μA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C

Typical Operating Characteristics

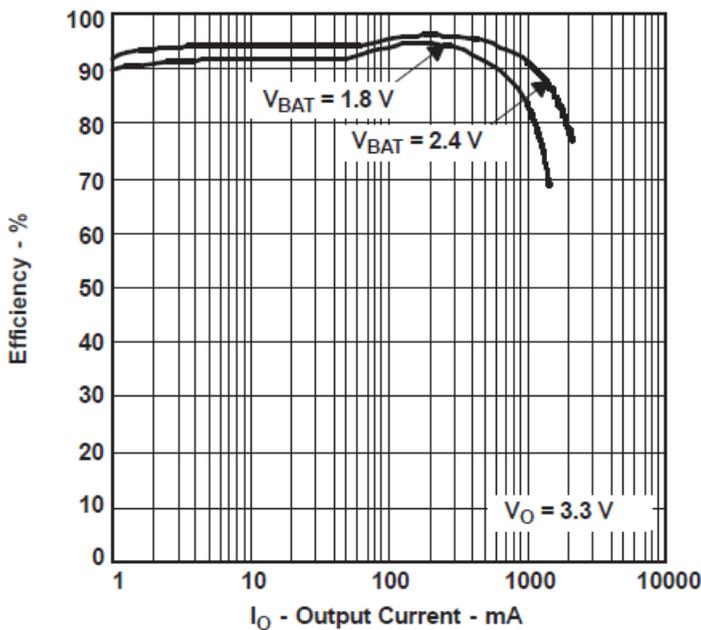
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE



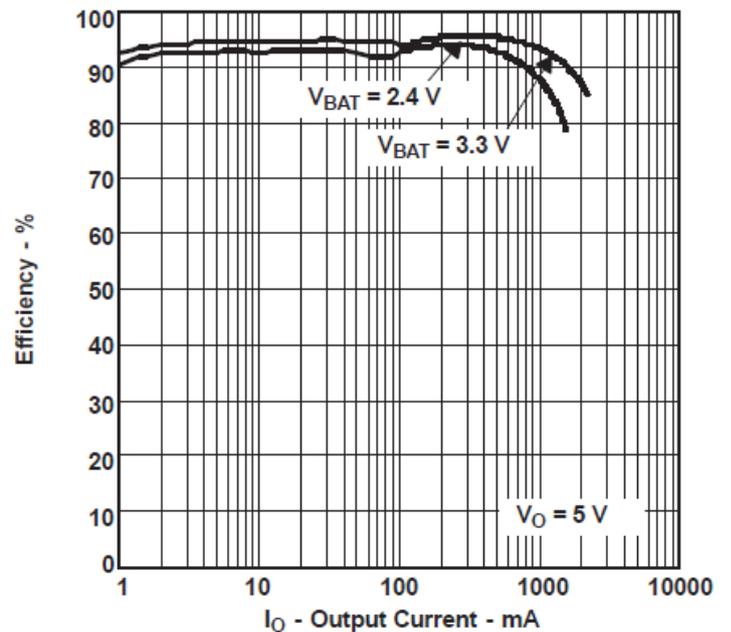
EFFICIENCY
vs
OUTPUT CURRENT



EFFICIENCY
vs
OUTPUT CURRENT

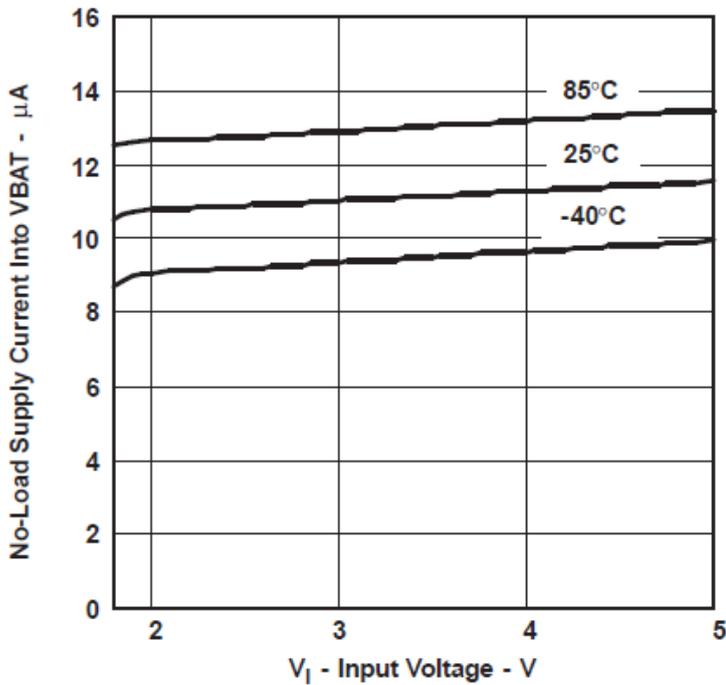


EFFICIENCY
vs
OUTPUT CURRENT

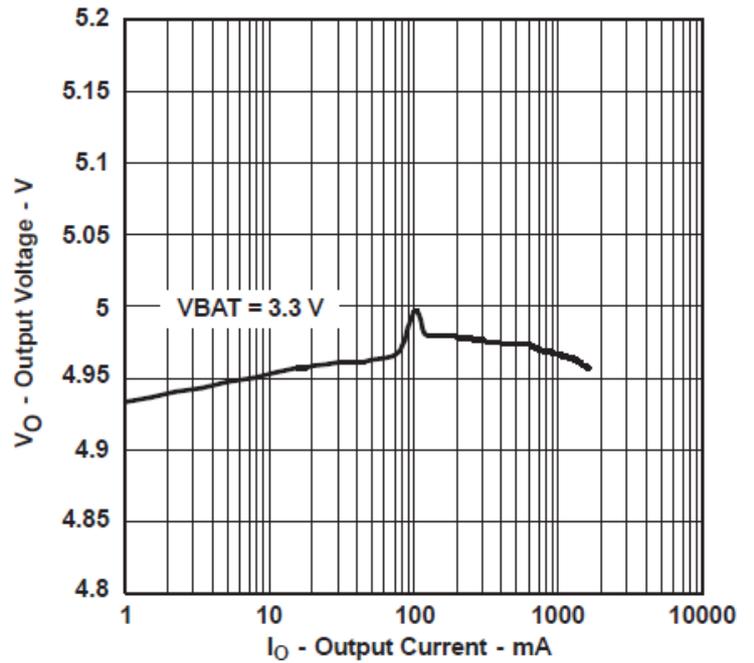


Typical Operating Characteristics(Cont.)

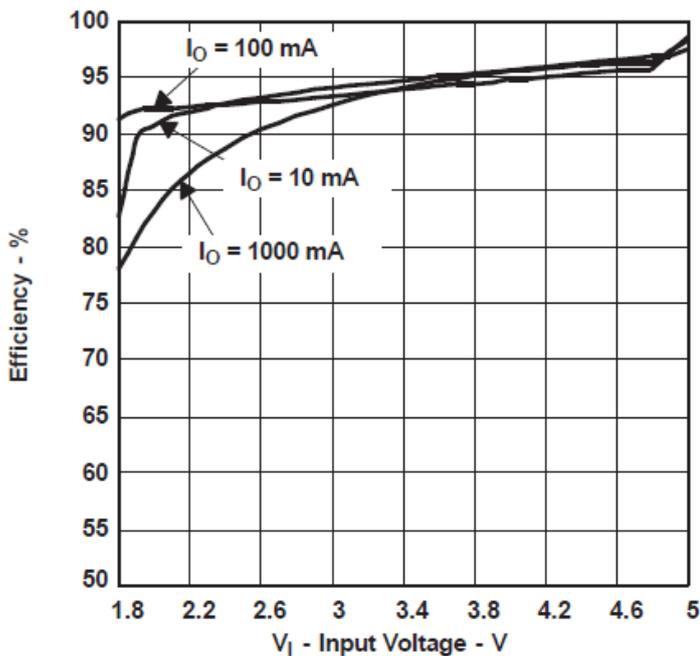
NO-LOAD SUPPLY CURRENT INTO VBAT
VS
INPUT VOLTAGE



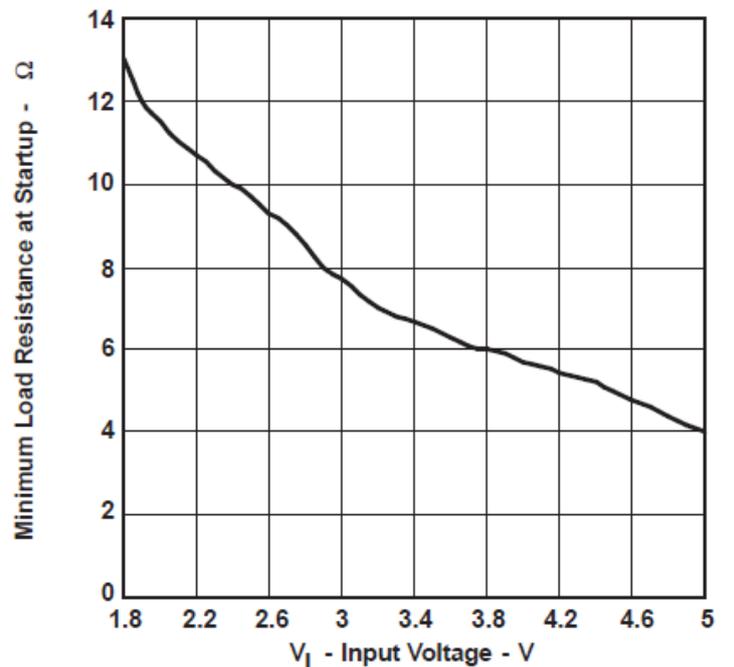
OUTPUT VOLTAGE
VS
OUTPUT CURRENT



EFFICIENCY
VS
INPUT VOLTAGE

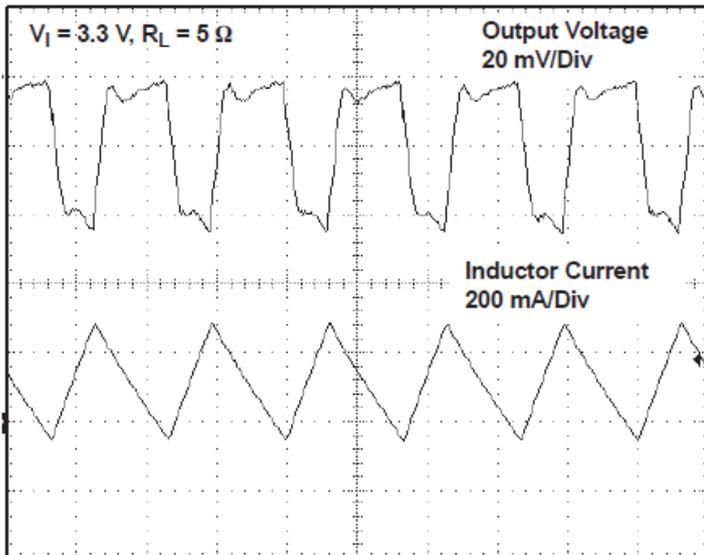


MINIMUM LOAD RESISTANCE AT START-UP
VS
INPUT VOLTAGE



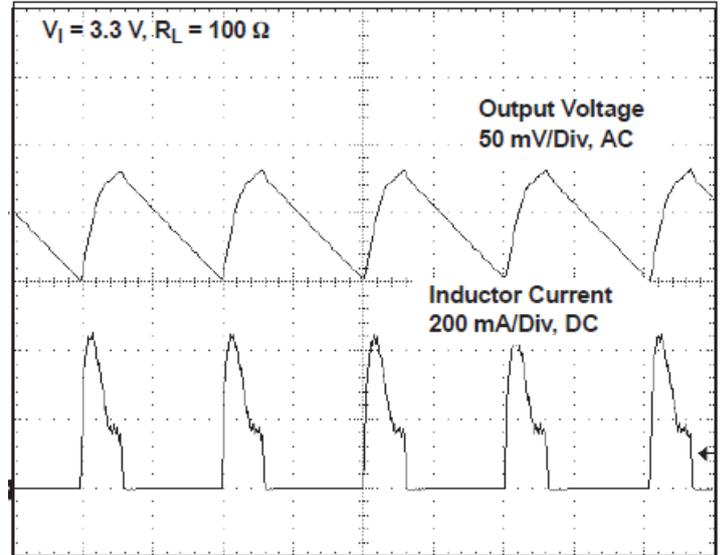
Typical Operating Characteristics(Cont.)

OUTPUT VOLTAGE IN CONTINUOUS MODE



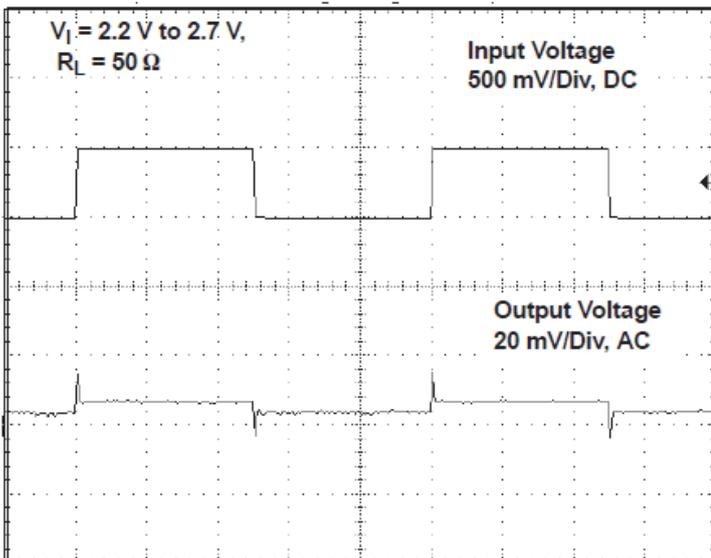
Timebase - 1 $\mu\text{s}/\text{Div}$

OUTPUT VOLTAGE IN POWER SAVE MODE



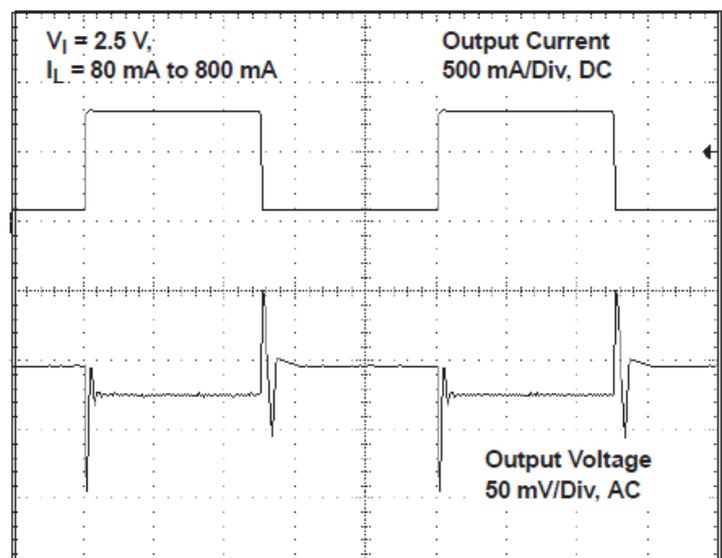
Timebase - 200 $\mu\text{s}/\text{Div}$

LINE TRANSIENT RESPONSE



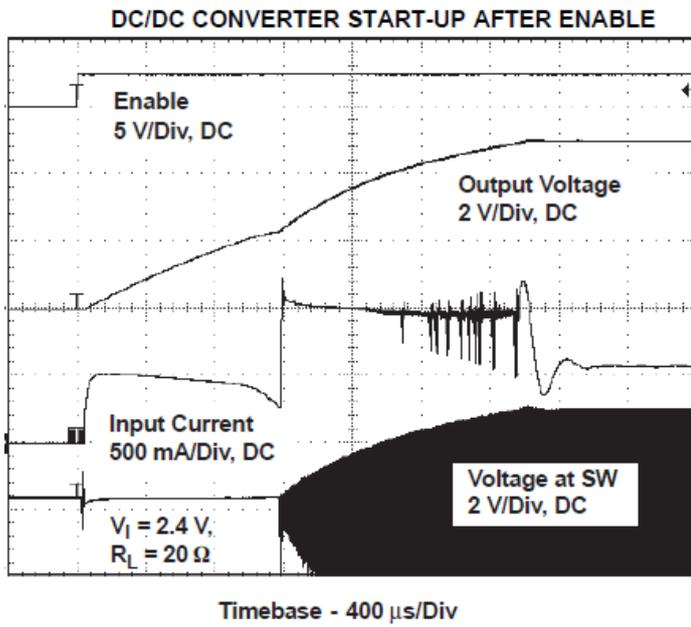
Timebase - 2 ms/Div

LOAD TRANSIENT RESPONSE

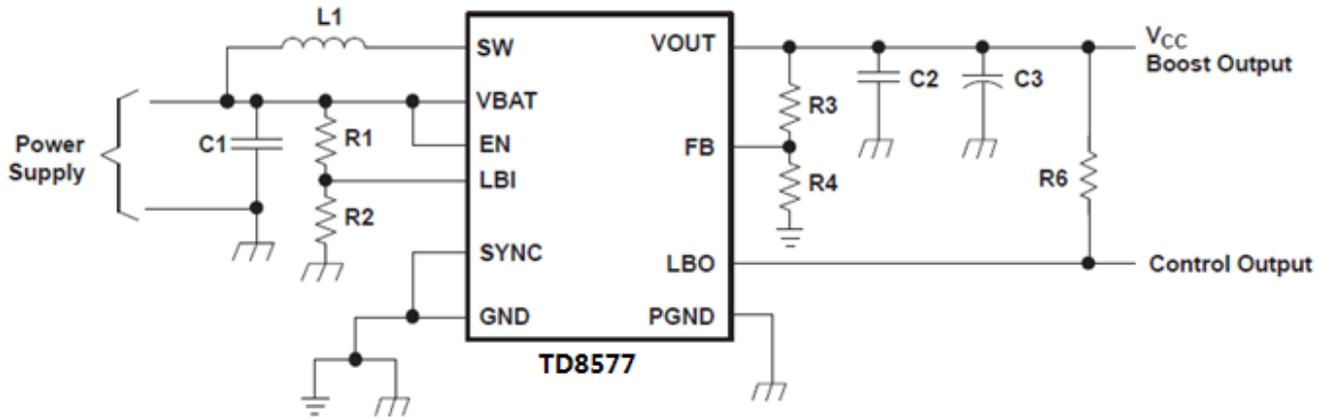


Timebase - 2 ms/Div

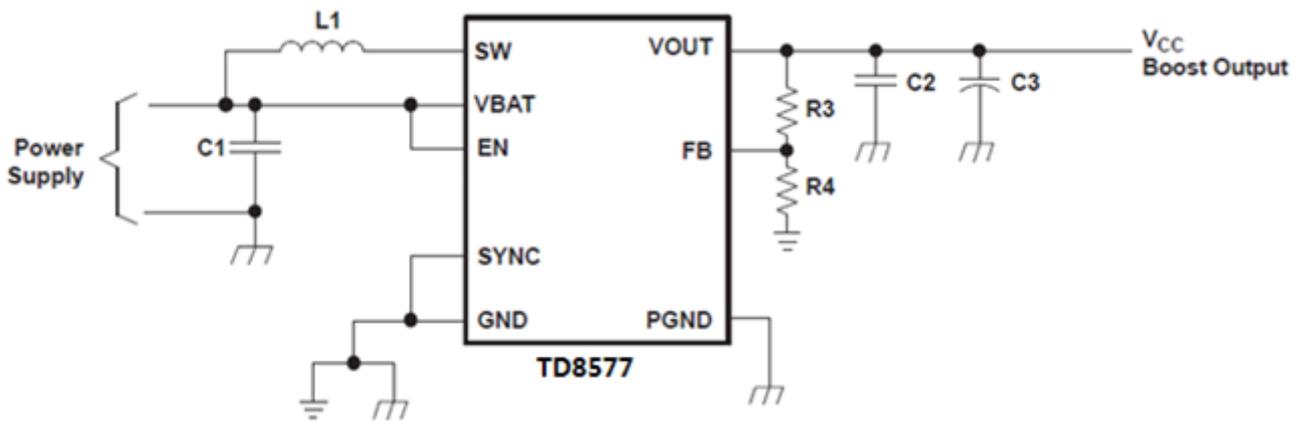
Typical Operating Characteristics(Cont.)



Type Application Circuit



TD8577 O/TD8577 V(TSSOP16/QFN-16)



TD8577 Q(DFN3*3-12)

Function Description

Controller Circuit

The controller circuit of the device is based on a fixed frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin or, at fixed output voltage versions, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 5000 mA. An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

Synchronous Rectifier

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 96%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low).

Synchronous Rectifier(Cont.)

The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the Synchronous Rectifier Section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VBAT is lower than approximately 1.6 V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 1.6 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

Softstart

When the device enables the internal start-up cycle starts with the first step, the precharge phase. During precharge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch current is limited in that phase. This also limits the output current under short-circuit conditions at the output. After charging the output capacitor to the input voltage the device starts switching. Until the output voltage is reached, the boost switch current limit is set to 40% of its nominal value to avoid high peak currents at the battery during startup. When the output voltage is reached, the regulator takes control and the switch current limit is set back to 100%.

Function Description(Cont.)

Power Save Mode and Synchronization

The SYNC pin can be used to select different operation modes. To enable power save, SYNC must be set low. Power save mode is used to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage. This power save mode can be disabled by setting the SYNC to VBAT. Applying an external clock with a duty cycle between 30% and 70% at the SYNC pin forces the converter to operate at the applied clock frequency. The external frequency has to be in the range of about $\pm 20\%$ of the nominal internal frequency. Detailed values are shown in the electrical characteristic section of the data sheet.

Low Battery Detector Circuit—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high-impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI threshold. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not let the LBI pin float.

Low-EMI Switch

The device integrates a circuit that removes the ringing that typically appears on the SW node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

Application Information

Design Procedure

The TD8577 dc/dc converters are intended for systems powered by a dual or triple cell NiCd or NiMH battery with a typical terminal voltage between 1.8 V and 5.5 V. They can also be used in systems powered by one-cell Li-Ion with a typical stack voltage between 2.5 V and 4.2 V. Additionally, two or three primary and secondary alkaline battery cells can be the power source in systems where the TD8577 is used.

Programming the Output Voltage

The output voltage of the TD8577 dc/dc converter section can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV. The maximum allowed value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 μ A, and the voltage across R6 is typically 500 mV. Based on those two values, the recommended value for R4 should be lower than 500 k Ω , in order to set the divider current at 1 μ A or higher. Because of internal compensation circuitry the value for this resistor should be in the range of 200 k Ω . From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using following equation:

$$R3 = R4 \times \left(\frac{V_O}{V_{FB}} - 1 \right) = 180 \text{ k}\Omega \times \left(\frac{V_O}{500 \text{ mV}} - 1 \right)$$

If as an example, an output voltage of 3.3 V is needed, a 1-M Ω resistor should be chosen for R3. If for any reason the value for R4 is chosen significantly lower than 200 k Ω additional capacitance in parallel to R3 is recommended. The required capacitance value can be easily calculated using following Equation :

$$C_{\text{par}R3} = 10 \text{ pF} \times \left(\frac{200 \text{ k}\Omega}{R4} - 1 \right)$$

Programming the LBI/LBO Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The

typical current into the LBI pin is 0.01 μ A, and the voltage across R2 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 500 mV. The recommended value for R2 is therefore in the range of 500 k Ω . From that, the value of resistor R1, depending on the desired minimum battery voltage V_{BAT} , can be calculated using following Equation:

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{LBI\text{-threshold}}} - 1 \right) = 390 \text{ k}\Omega \times \left(\frac{V_{BAT}}{500 \text{ mV}} - 1 \right)$$

Programming the LBI/LBO Threshold Voltage(Cont.)

The output of the low battery supervisor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 M Ω . The maximum voltage which is used to pull up the LBO outputs should not exceed the output voltage of the dc/dc converter. If not used, the LBO pin can be left floating or tied to GND.

Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TD8577's switch is 4500 mA at an output voltage of 5 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using following Equation:

$$I_L = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8}$$

For example, for an output current of 1000 mA at 5 V, at least 3500 mA of average current flows through the inductor at a minimum input voltage of 1.8 V.

Application Information(Cont.)

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs. With those parameters, it is possible to calculate the value for the inductor by using following Equation:

$$L = \frac{V_{BAT} \times (V_{OUT} - V_{BAT})}{\Delta I_L \times f \times V_{OUT}}$$

Parameter f is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., $10\% \times I_L$. In this example, the desired inductor has the value of $5.5 \mu\text{H}$. In typical applications a $6.8 \mu\text{H}$ inductance is recommended. The minimum possible inductance value is $2.2 \mu\text{H}$. With the calculated inductance and current values, it is possible to choose a suitable inductor. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in equation 4. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers have been used with the TD8577 converters:

VENDOR	INDUCTOR SERIES
Sumida	CDRH124
	CDRH103R
	CDRH104R
Würth Elektronik	7447779
	744771
EPCOS	B82464G

Input Capacitor

At least a $10\text{-}\mu\text{F}$ input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended.

Output Capacitor

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using following Equation:

Output Capacitor(Cont.)

$$C_{\min} = \frac{I_{OUT} \times (V_{OUT} - V_{BAT})}{f \times \Delta V \times V_{OUT}}$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10 mV , a minimum capacitance of $100 \mu\text{F}$ is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using following Equation:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR}$$

An additional ripple of 80 mV is the result of using a tantalum capacitor with a low ESR of $80\text{ m}\Omega$. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 90 mV . Additional ripple is caused by load transients. This means that the output capacitance needs to be larger than calculated above to meet the total ripple requirements.

The output capacitor must completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change. With the calculated minimum value of $100 \mu\text{F}$ and load transient considerations, a recommended output capacitance value is in around $220 \mu\text{F}$. For economical reasons this usually is a tantalum capacitor. Because of this the control loop has been optimized for using output capacitors with an ESR of above $30\text{ m}\Omega$. The minimum value for the output capacitor is $22 \mu\text{F}$.

Application Information(Cont.)

Small Signal Stability

When using output capacitors with lower ESR, like ceramics, it is recommended to use the adjustable voltage version. The missing ESR can be easily compensated there in the feedback divider. Typically a capacitor in the range of 10 pF in parallel to R3 helps to obtain small signal stability with lowest ESR output capacitors. For more detailed analysis the small signal transfer function of the error amplifier and regulator, which is given in following Equation, can be used.

$$A_{REG} = \frac{d}{V_{FB}} = \frac{5 \times (R3 + R4)}{R4 \times (1 + i \times \omega \times 2.3 \mu s)}$$

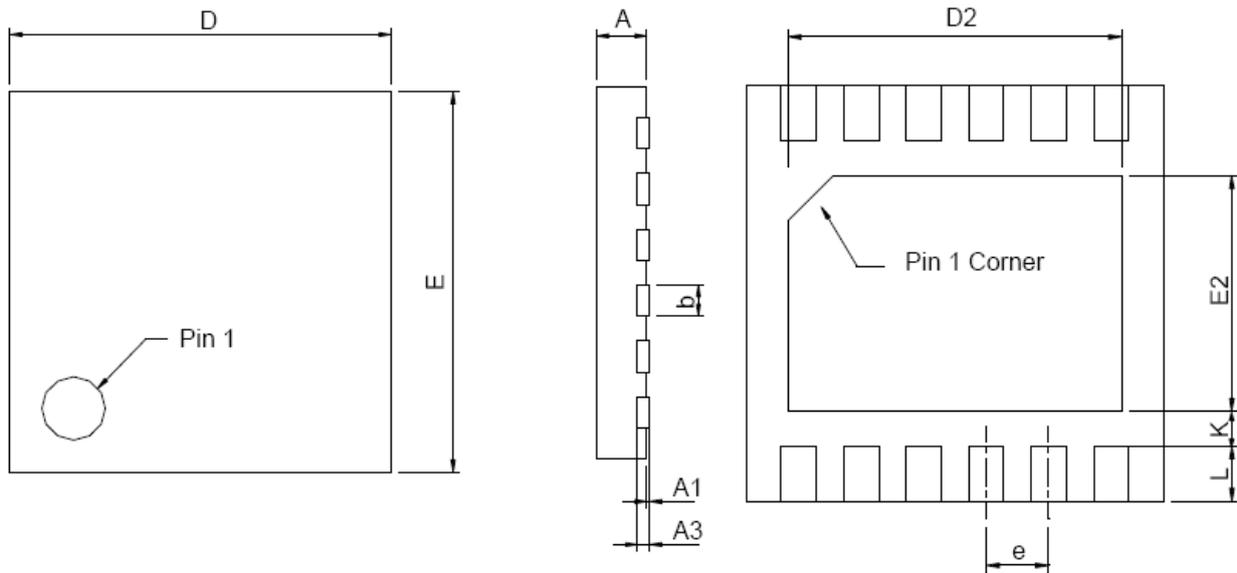
Layout Considerations

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

Package Information

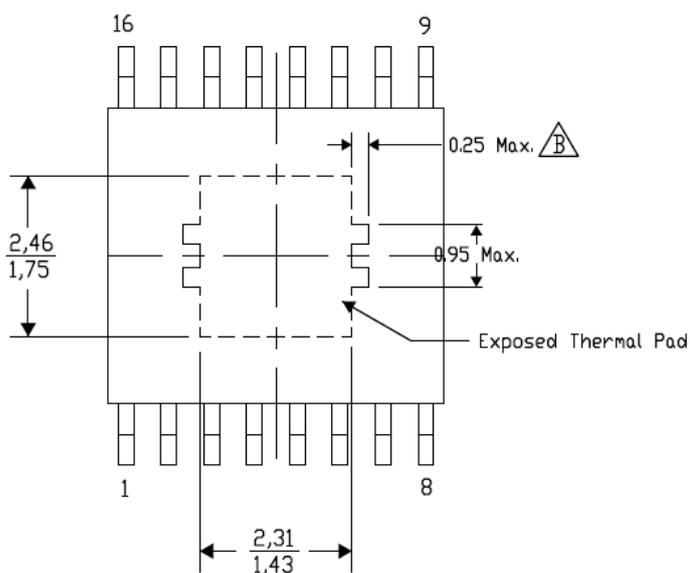
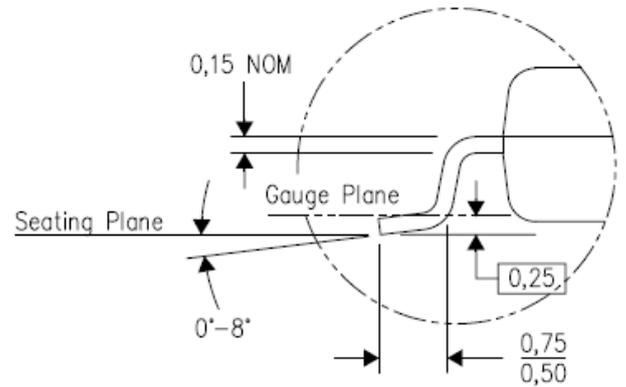
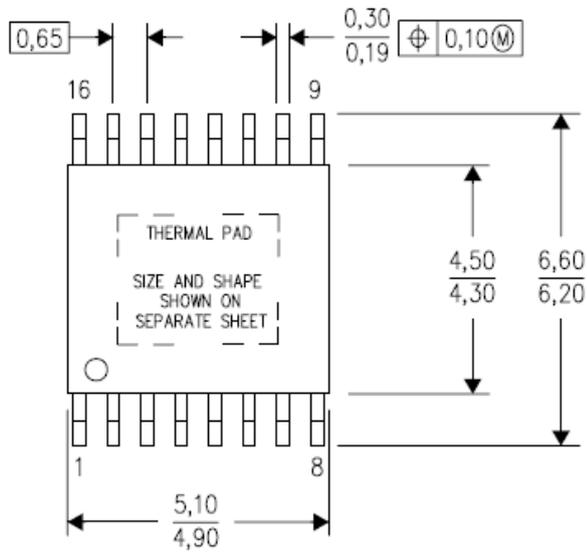
DFN3x3-12



SYMBOL	DFN3x3-12			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.45 BSC		0.018 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

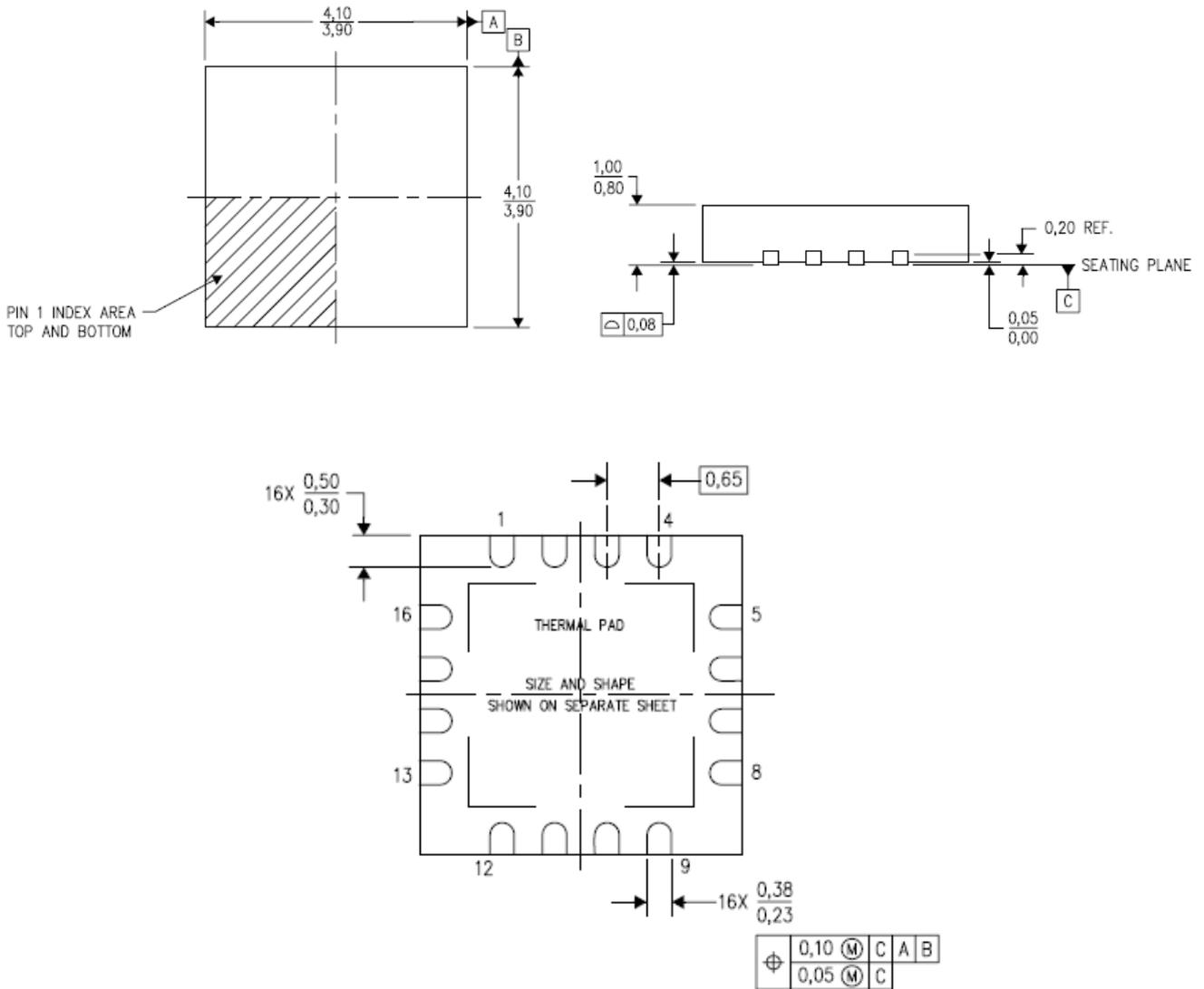
Package Information(Cont.)

TSSOP-16



Package Information(Cont.)

QFN-16



Design Notes